High Speed Interface Techniques for Computer Peripherals

Workshop High Speed Interconnects
Universität Stuttgart INT
07. November 2008

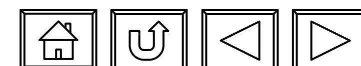
Dr.-Ing. Peter Gregorius

Peter.Gregorius@qimonda.com

Peter.Gregorius@int.uni-stuttgart.de

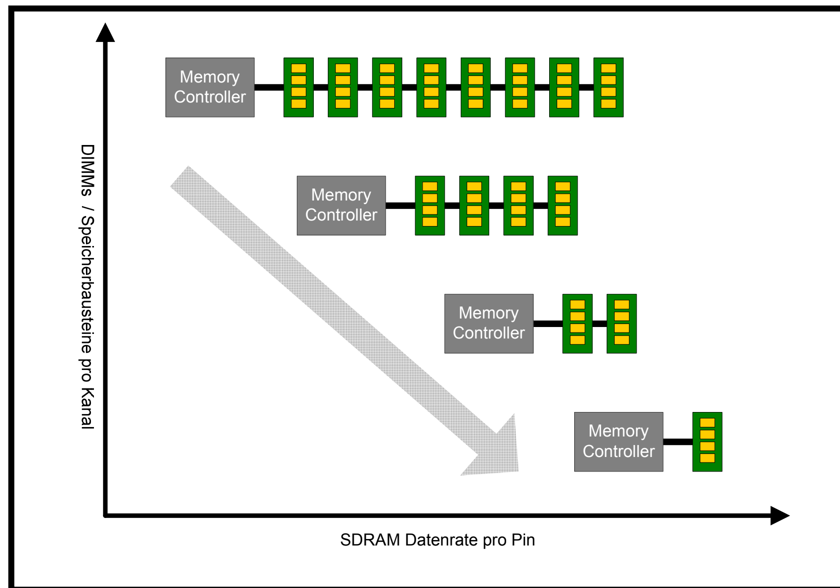
High Speed Interface Techniques

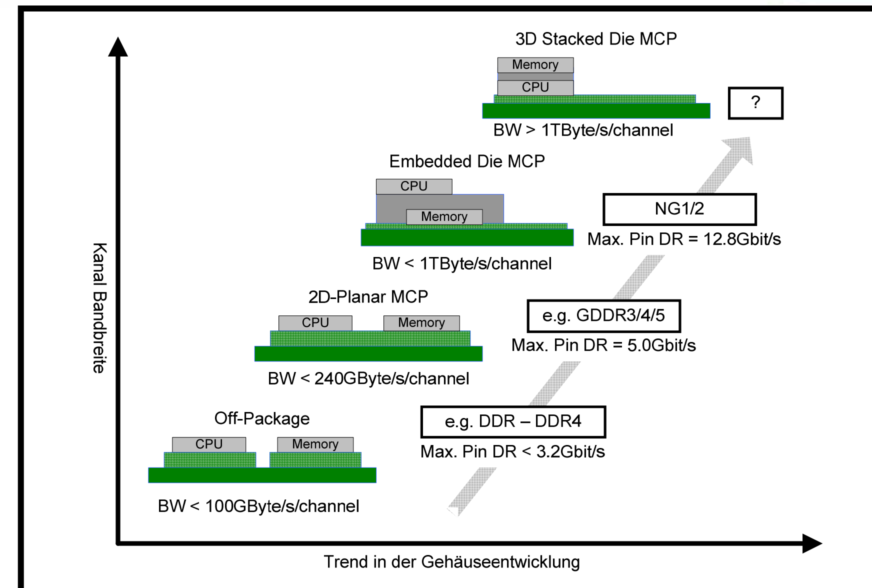
- Introduction, Trends and Limitations
- Review on Cascading Techniques (ISSCC2007)
- Clocking
- Outlook & Summary



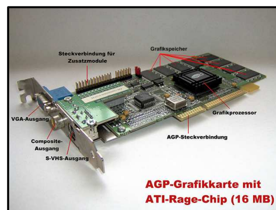
Confidential

Computer Peripherals I/O-Trend

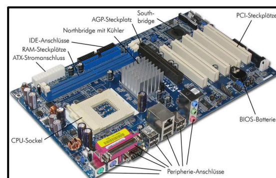




High Performance Graphic Memory



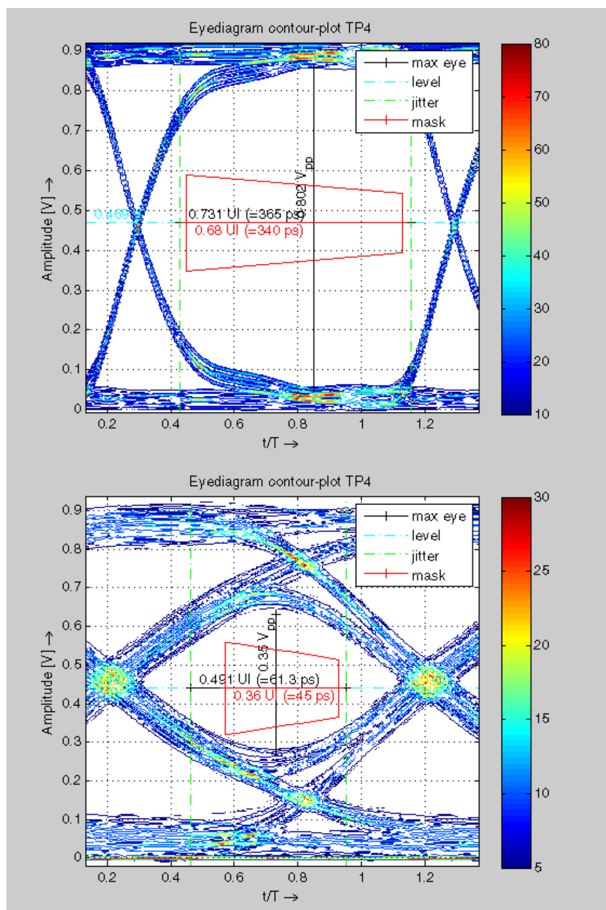
High Performance PC Memory



Memory Roadmap – Signaling

Example: GDDR5 / 2D planar chip-to-chip

Example: DDR4 (under discussion) / dual slot



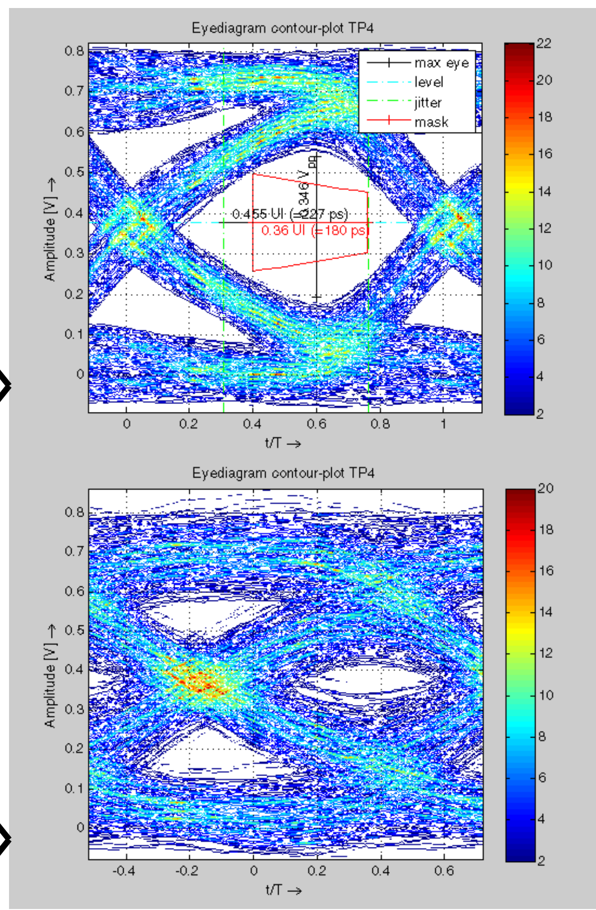
Conditions:
1. SE signaling, at nominal supply voltage (1.5V)
2. No power supply noise
3. Physical BER=10^{-12}
4. 4 Layer PCB

2Gbit/s/pin
T_{UI}= 500ps
T_{eye}= 340ps

2Gbit/s/pin
T_{UI}= 500ps
T_{eye}= 180ps

8Gbit/s/pin
T_{UI}= 125ps
T_{eye}= 45ps

3.2Gbit/s/pin
T_{UI}= 312.5ps
T_{eye}= -



Note: SE signaling, channel data contains worst-case cross-talk and is based on actual board design.

Pin count, channel bandwidth and data rate

Memory I/O Evolution

Normaized channel bandwidth [GByte/s]: 2^7, 2^6, 2^5, 2^4, 2^3, 2^2, 2^1, 2^0, 0

Normaized data pin count: 8, 6, 4, 2, 0

Northbirdge

~150 Signals

DIMM

DIMM

SE Off Package Limit ~ 2.6Gbit/s (BER=10^{-12})

DS Off Package Limit ~ 12Gbit/s (BER=10^{-12})

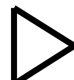
Standard ► DDR1 200 (BOL) · DDR1 400 (EOL) · DDR2 400 (BOL) · DDR2 800 (EOL) · DDR3 800 (BOL) · DDR3 1600 (EOL) · DDR4 1600 (BOL) · DDR4 3200 (EOL) · NG1 3200 (BOL) · NG1 6400 (EOL) · NG2 6400 (BOL) · NG2 12800 (EOL) · ?

► For the last decade the effective (DQ) data pin count remains constant. The evolution in data rate and bandwidth was based on the increase in frequency!

►Following the bandwidth roadmap in 2012/13 single ended signaling will hit a wall (signal + power integrity!)

►Differential signaling (DS) may give room for one or two generations but means a stop of the (G)DDRx evolution.

Key Requirements for Memory Subsystem



BW, Speed, Latency (GByte/s, Mbit/s, ns)	Density (Gbit)	Power (mW)	Cost ($$$)

Solution for high density - FBDIMM

FBDIMM: Fully Buffered Dual Inline Memory Module

DDR2 IO [Mb/s]	400	533	667	800
AMB IO [Gb/s]	2.4	3.2	4.0	4.8

2.4Gbit/s/Lane –
4.8Gbit/s/Lane

Southbound (SB)

Northbound (NB)

North Bridge

10

14

DRAM

RX TX AMB TX RX

200, 266, 333
and 400MHz

PLL

AMB:
Advanced
Memory Buffer

DDR2
Connector

Southbound (SB)

Northbound (NB)

Connector

TX_S[9:0]

RX_P[9:0]

REF_CLK

TX_P[13:0]

RX_S[13:0]

DQ

CA

I/O

RX

TX

DRL

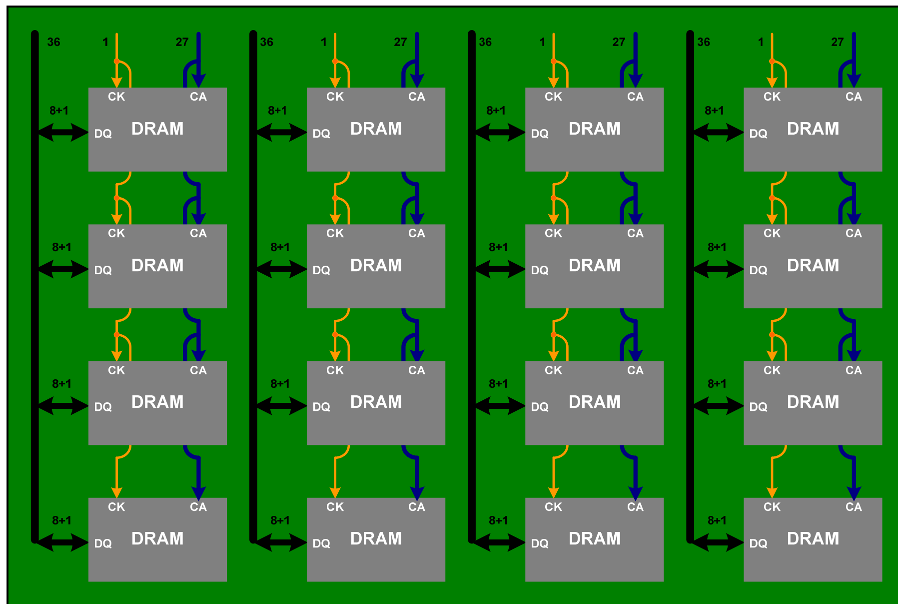
PLL

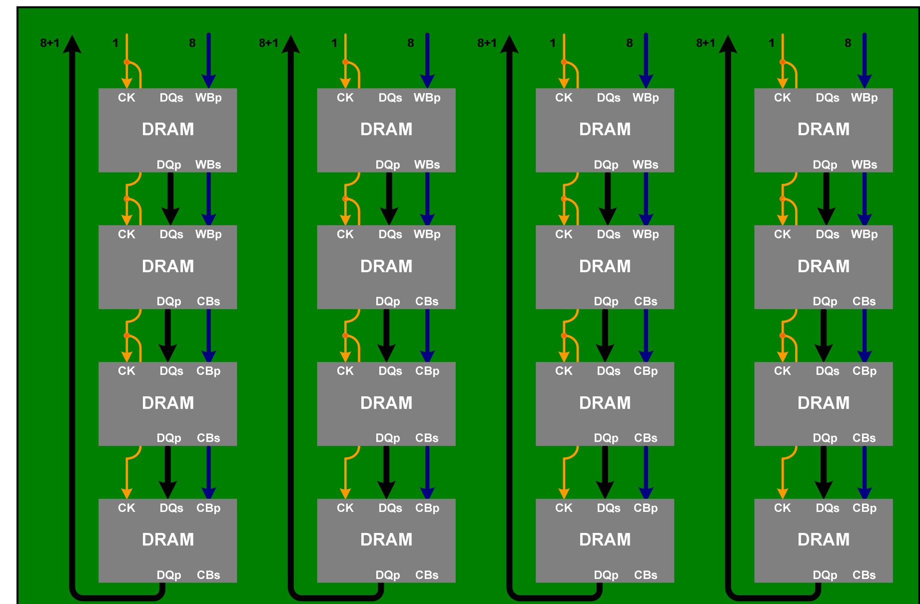
Data Bus Interface

Source: N.Dadalt, P.Gregorius, E. Thaller, L. Gazsi; "A Compact Triple-Band Low Jitter Digital LC PLL with Programmable Coil in130nm CMOS," IEEE Solid State Circuit Journal, June 2005

Alternative Approach: repeater DRAM

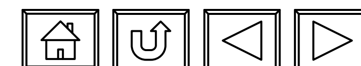
DIMM with multi-drop connections	DIMM with repeater DRAMs





- high pin count (DDR2 SO DIMM =204pins)
- parallel interface
- bidirectional single ended DQ (data bus)
- uni-directional single ended CA bus

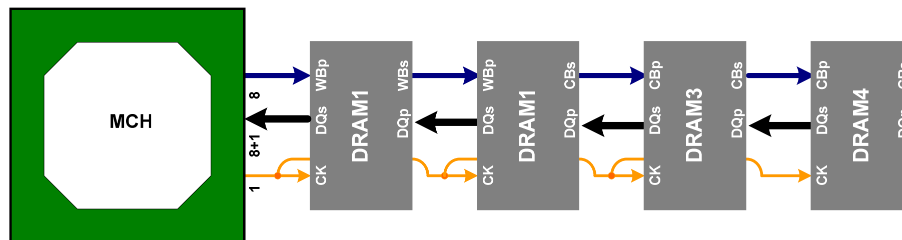
- lower pin count
- serial interface (frame based)
- differential signaling
- simultaneous READ / WRITE



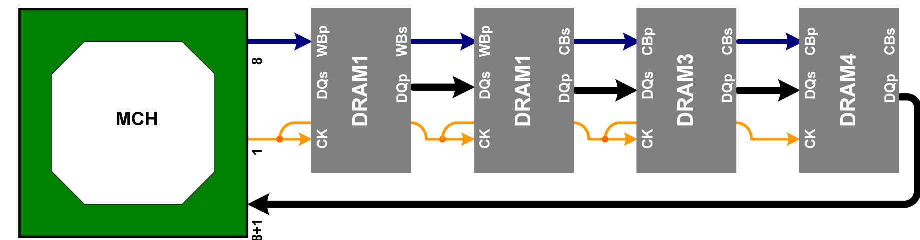
Confidential

Repeater Topologies

Loop Back Topology (FBDIMM)



Loop Forward Topology



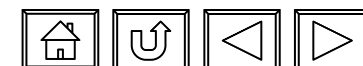
Embedded Command/Address WRITE bus

Coded READ bus with seamless data insertion

Differential P2P Connections

READ / WRITE latency depends on DRAM position within daisy chain
➔ needs HS FIFO

READ + WRITE latency = const.
➔ better to control for MCH



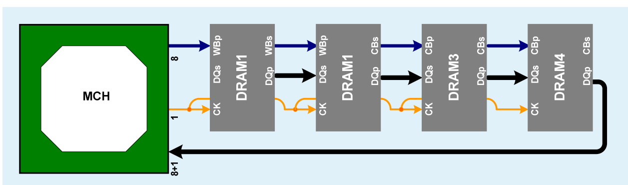
Confidential

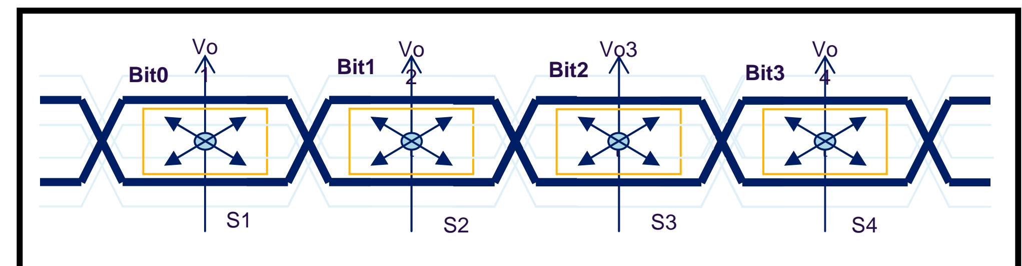
Repeater DRAM Test Chip – HS IO Section

transparent repeat

re-sample path

RT RT RT RT
RxP RxN TxP TxN
RX RX RX TX
DzP DzN DxP DxN
SEL
4 Data
4 CLK
Sampler Unit
4x
P2S
CTL_P2S
S1 S2 S3 S4
CrP CrN CtP CtN
CiP CiN
IQ DIV
Tree
PI
CTL_PI





Sampler Eye Characterization

6.5mm
DATA
CLK
L6 L5 L4 L3 L2 L1 CL
1cm

Bit0 Bit1 Bit2 Bit3

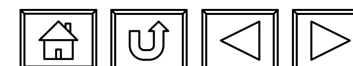
receiver offset shmoo -200mV...+200mV

~66ps
~105ps
~108ps
~83ps

phase interpolator setting shmoo 0-360°(60 steps)

Data Rate = 4.8Gbit/s/lane (UI=208ps) / Accumulated Eye over 6 Lanes – Transparent Mode

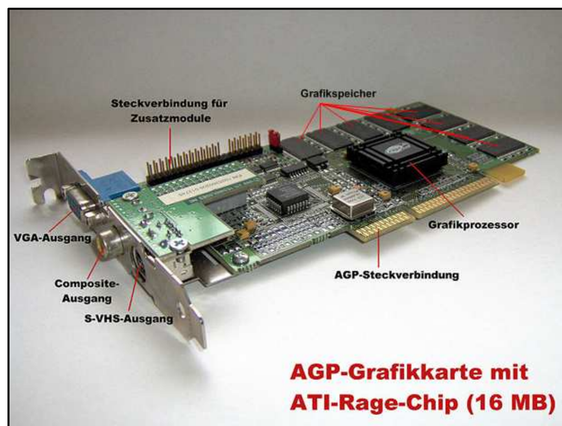
Source: Z. Gu, P. Gregorius, D. Kehrer, L. Neumann, T. Rickes, H. Ruckerbauer, R. Schledz, M. Streibl, etc.; "Cascading Techniques for a High-Speed Memory Interface, "IEEE International Solid State Circuit Conference, Session 12.7, Februar 2007



Intermediate Summary

► Proposed technique solves density, pin count and power requirements for future architectures.

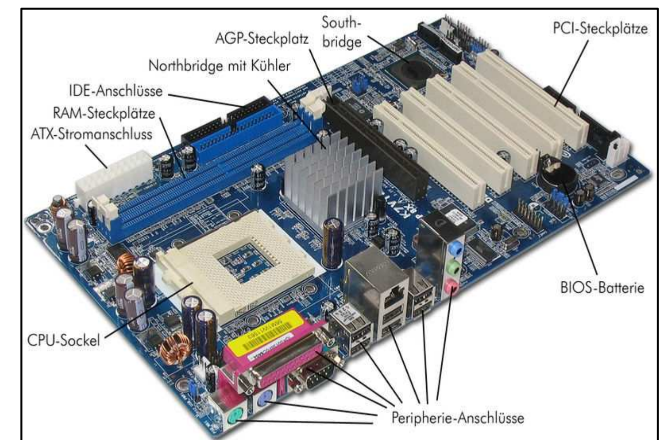
► Limitations in physical link remains



4 Layer PCB signaling limit

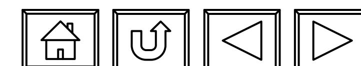
◄SE 2D Planar ~10Gbit/s/pin
◄DS 2D Planar ~18Gbit/s/pin

SE 2D Planar ~2.6Gbit/s/pin ►
DS 2D Planar ~12Gbit/s/pin ►



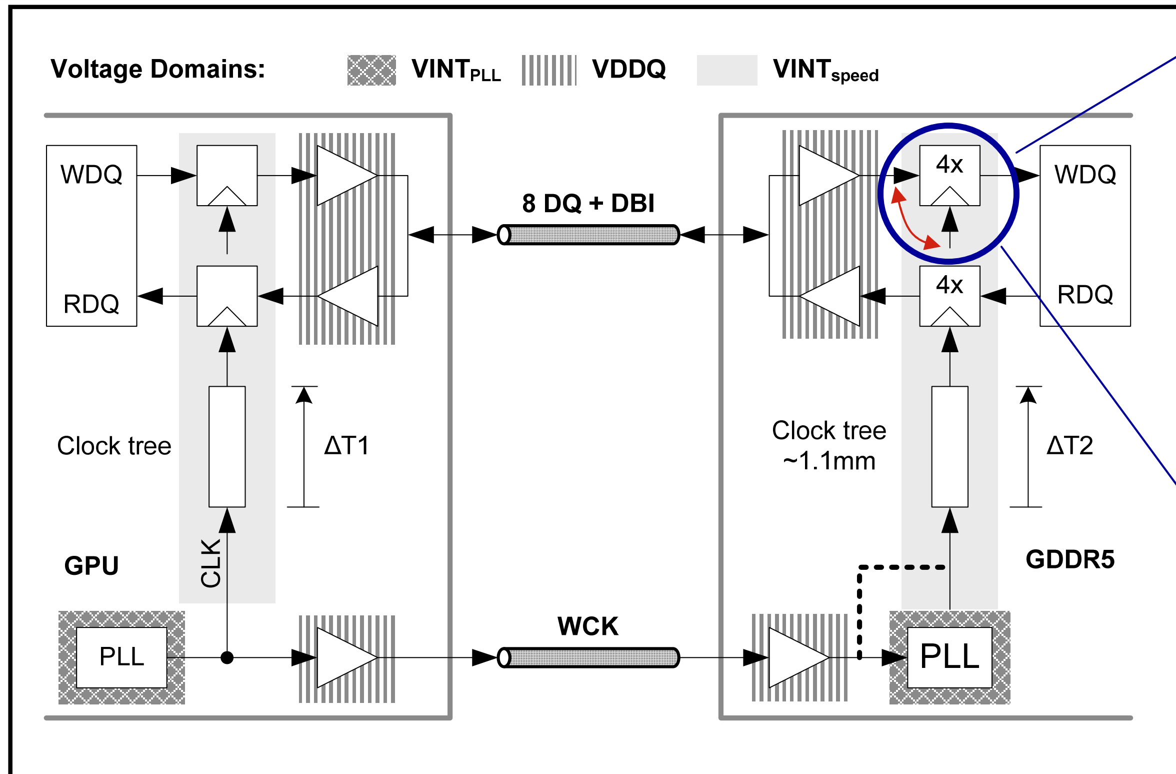
► DRAM roadmap doesn‘t follow CPU (nCore) BW requirement

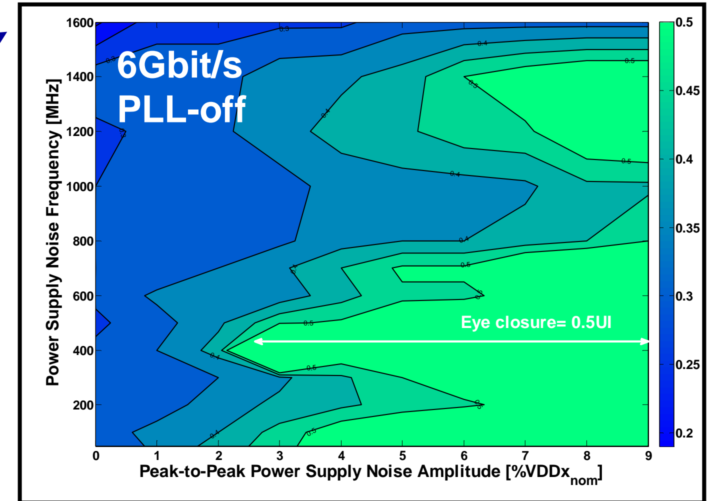
► Clock and data distribution needs complex link training
► Power consumption, testability etc.



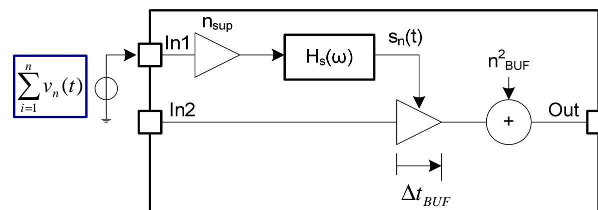
Confidential

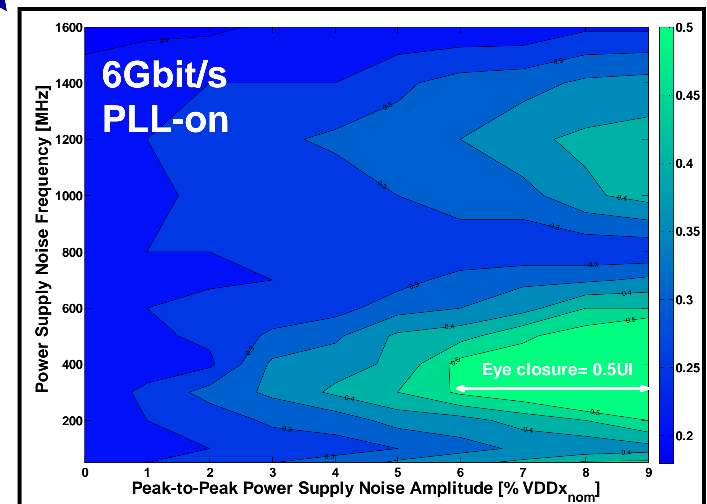
GDDR5 Power Integrity ◄► Signal Integrity





Power Supply Sensitivity Model





Confidential

Impact of Clock Path Device Mismatch

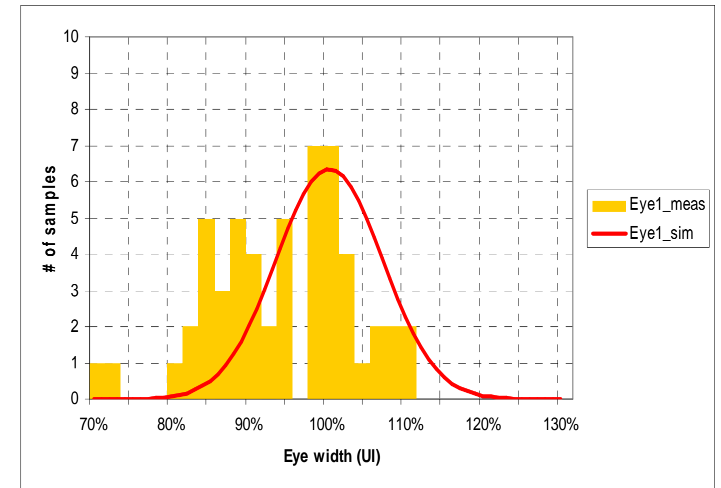
500
0
-500
Transparent repeat mode

500
0.94 UI 1.03 UI 1.03 UI 1.00 UI
0
-500
Resample mode (typical mismatch)

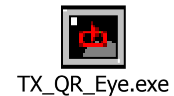
500
1.16 UI 0.99 UI 0.86 UI 0.99 UI
0
-500
Resample mode (large mismatch)

Eye Diagram Voltage, mV

100ps/div

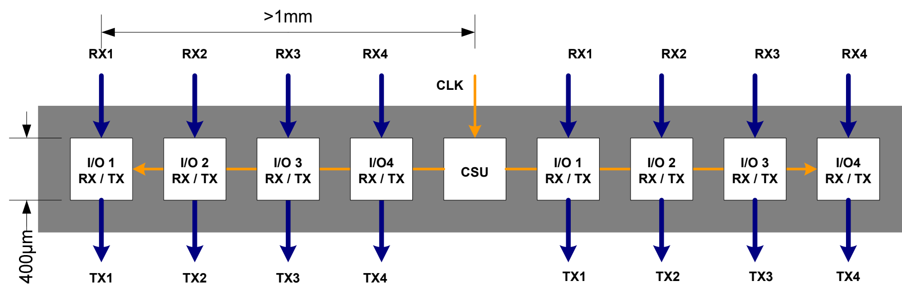


standard deviation = 9%·UI
(7%·UI from the clock generator)



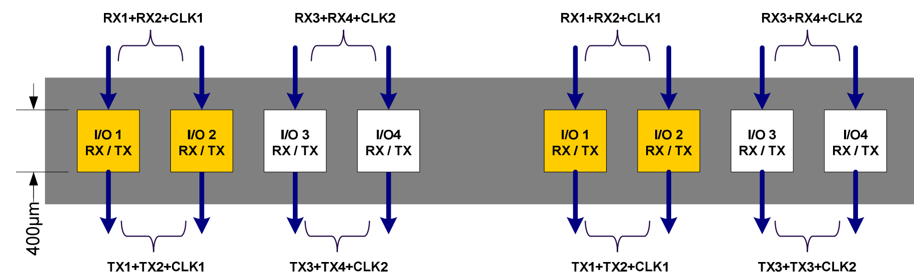
Ghost Signaling Motivation

Standard On-Chip Clocking

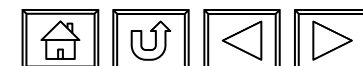


- phase matching problem for on-chip QR sampling clock
- needs complex bit wise data training
- distributed timing recovery (MCH ↔ DRAM)
- signal integrity is difficult no good scalability

Ghost Signaling



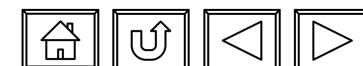
- clock distributed together with data
- source synchronous
- no distributed timing recovery needed
- no internal clock tree
  - save power, less complex
- good scalability
- pin count reduced
- improved signal integrity (no sampling phase problems)



Confidential

Ghost Signaling Repeater High Speed I/O

VSUP+
RT RT
RxP
RxN
RX
DiN
DiP
C R R C
CiN
CiP
DzP
DzN
SEL
CTL_P2S
2 Data
2 CLK
Sampler Unit 2x
S1 S2
P2S
DxP
DxN
D0P
D0N
D1P
D1N
TX
TxP
TxN
CoN
CoP
BUF
CxP
CxN



Confidential

Summary

High Density Solutions (e.g. Server)

→ FBDIMM / DDR2; Advanced Memory Buffer, Differential Signaling 2.4Gbit/s – 4.8Gbit/s

→ RDIMM / DDR3; Single Ended Point-to-Point or Point-to-2 Point ~2Gbit/s max

→ Buffer-on-Board / NG DRAM with Repeater, Differential Signaling 4.8Gbit/s – 9.6Gbit/s

Ultra High Bandwidth (Graphic)

→ GDDR5; Single Ended Point-to-Point up to ~10Gbit/s

→ GDDR6; 3D Integration Single Ended ~10Gbit/s but x2 Pin count (x64 DRAM)

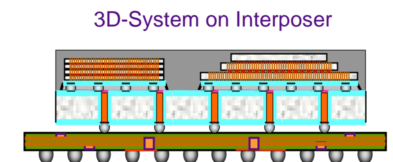
→ Buffer-on-Board / DDR3 / DDR4(?); Differential Signaling 4.8Gbit/s – 9.6Gbit/s

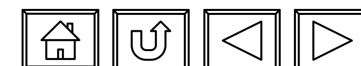
High Bandwidth with 'moderate' Power (Notebook)

→ DDR4, Single Ended Dual Slot up to 2.4Gbit/s or Point-to-Point ~3Gbit/s

→ Ultra Parallel Single Ended 3D Integration up to 2Gbit/s

3D-System on Interposer





Thank you

The World's Leading
Creative Memory Company