Continuous-Time Bandpass Delta-Sigma Modulator for a Signal Frequency of 2.2 GHz

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Abstract—A continuous-time bandpass delta-sigma modulator (CT BPDSM) for class-S power amplifier applications with a center frequency of 2.2 GHz is presented. Class-S amplifiers are considered to provide a very power efficient way to amplify signals with high dynamic range. The modulator has a multi-feedback architecture. It features a low noise transconductor with series emitter degeneration, tunable LC resonators with Q-enhancement and an optimized clock tree operating at 7.5 GHz. The circuit is implemented in a 200 GHz-f_T SiGe-bipolar technology. A peak SNDR of 43 dB in a bandwidth of 20 MHz is measured. The circuit dissipates 450 mW from a 3.6 V supply.

Keywords- Delta-sigma modulator, class-S power amplifier, bipolar integrated circuit.

I. INTRODUCTION

Power amplifiers (PA) for base stations require high linearity and high output power at good power efficiency. With the advent of modern multiplexing schemes, such as code division multiple access (CDMA) and orthogonal frequency division multiple access (OFDMA), the peak to average power ratio (PAPR) of the transmitted RF signal has grown considerably. This leads to a significant loss in power efficiency for standard class-AB PAs.

One possible replacement for the conventional class-AB power PA is the class-S amplifier [1]. One realization consists of a switching-mode amplifier, a CT BPDSM and finally a reconstruction filter. The CT BPDSM generates a fast alternating bitstream from the analog RF signal. The digital output signal of the modulator is amplified by the switching-mode PA. Then, the desired RF signal is reconstructed with a high-Q bandpass filter. The concept can be included in a conventional RF transmission chain like in Fig. 1. Only the filter and the power amplifier have to be replaced by the class-S amplifier.

This work describes the CT BPDSM which plays a key role in the concept. The paper is organized as follows: In Section II the system architecture and the main components of the modulator are described. Measurement results are discussed in Section III and conclusions are given in section IV.

II. DESIGN

A. System architecture

The synthesis of CT BPDSM can be done with the aid of a discrete-time model. At the sampling instance this model is isomorphic to the continuous-time modulator. Many implementations are based on the fourth order double loop structure [2,3]. However, a direct impulse-invariant transform with a Non-Return-to-Zero (NRZ) DAC in the feedback path does not lead to a realization with a simple 2nd order bandpass filter [4]. The introduction of another feedback pulse into each summation node eliminates this problem. A set of Return-to-Zero (RZ) and Half-Return-to-Zero (HRZ) feedback pulses is easy to implement for high frequencies and therefore chosen for this circuit [5].
A block diagram of the modulator is depicted in Fig. 2. The modulator consists of two Q-enhanced LC resonators. They are fed with three currents: The first is proportional to the input voltage of the preceding transconductor $G_m$. The other two are feedback currents with DAC amplitudes of $k_{xr}$ and $k_{xh}$ during the HIGH output of the RZ latch and HRZ latch, respectively.

The sign of the feedback current is determined by the sampling comparator. The RZ branch exhibits one digital half delay, the HRZ branch one full delay compared to the comparator output. To avoid metastability of the output signal the signal is resampled and amplified by two latches at the output.

B. Circuit components

Fig. 3 shows the employed transconductor topology for $G_m$ and $G_q$. The emitter follower at the input increases the input impedance and decouples the resonators from each other. The series emitter degeneration improves the linearity. The output noise with series degeneration is lower than with shunt degeneration. With shunt degeneration, the noise currents of the two current sources couple into the two complementary outputs separately. With series degeneration, the current source noise converts to common mode noise and does not have effect on the output current difference. The simulated difference in noise power is 4.6 dB, this justifies the slightly larger supply voltage requirement of the series degenerated transconductor.

The resonator consists of a parallel resonant circuit with two inductors, a differential capacitor and a tunable differential varactor-capacitor. The poor Q-factor of the on-chip inductor is enhanced by an active negative conductor $G_q$ which has the same topology as $G_m$. The comparator consists of a preamplifier and two latches. The clock tree is signal flow oriented. To compensate for excess-loop-delay the comparator clock is delayed with respect to the last feedback latches.

III. EXPERIMENTAL RESULTS

The modulator is designed in a 200 GHz-$f_t$ SiGe-HBT process (B7HF200) from Infineon. The circuit occupies an area of 1.8 mm$^2$. A chip microphotograph is shown in Fig. 4. It consumes 450 mW from a 3.6 V supply including clock tree and output drivers.

Two 180° hybrid couplers are used in the measurement setup for single-ended-to-differential conversion. The first one for the signal input and the other one for the 7.5 GHz clock input. A third 180° hybrid coupler converts the differential output to a single-ended signal. A wideband UMTS-FDD CDMA input signal is provided by a Rohde&Schwarz SMA 200A. Spectrum and error-vector-magnitude (EVM) measurements are done with a Rohde&Schwarz FSQ 8.

Fig. 5 shows the measured output eye diagram. The 50 Ω output driver provides for complementary output signals with a single-ended voltage swing of 300 mV. The jitter generation of the whole modulator is below 1 ps. The modulator output spectrum from dc to 7.5 GHz is depicted in Fig. 6.
As the noise power density in the notch is almost flat in a bandwidth of at least 60 MHz around the signal peak, the noise floor power can be determined by multiplying the measured noise power density with the considered signal bandwidth.

Fig. 7 shows the modulator output signal power and noise power in different bandwidths versus the input power. The input referred 1-dB compression point $P_{in,1dB}$ is at -8 dBm. The change from the linear to the saturated characteristic is very abrupt. It occurs when the DAC feedback currents are too small to compensate for the currents that are generated by the input transconductors $G_m$. The output signal disappears for an input power smaller than -44 dBm. This behavior is caused by the offset of the comparator. The switching threshold of the comparator is some millivolt offset from the quiescent state of the resonator. Thus neither the resonator noise nor a very small input signal is capable to start the switching action of the modulator.

The signal-to-noise ratio (SNR) is plotted versus the input power in Fig. 8. The maximum SNR for non-saturated operation is achieved for an input power that is 1 to 6 dB lower than $P_{in,1dB}$. The maximum SNR is 52 dB for 4 MHz bandwidth, 45 dB for 20 MHz and 40 dB for 60 MHz bandwidth.

Third order intermodulation is measured with a two-tone input signal. The combined output power of the fundamental tones and of the 3rd order intermodulation tones is plotted versus the combined power of the input tones in Fig. 9. As the peak envelope power (PEP) of a two-tone signal is 3 dB larger than the average power, the modulator saturation effects already occur at an input power that is 3 dB smaller than $P_{in,1dB}$. This is indicated in Fig. 9: a very steep increase of the 3rd order intermodulation can be observed at this point.
The uncommon increase of intermodulation with decreasing signal power is also attributed to the comparator offset, as this behavior coincides with the output power disappearance at small input power. The common region of the 30 dB/decade-slope of the 3rd order intermodulation products is covered by the saturation and by the comparator offset effects for large and small input power, respectively. Nevertheless, 3rd order harmonic distortion is more than 40 dB lower than the corresponding output power is -10 dBm. The ACLR at 5 MHz offset is mainly limited by intermodulation, and the fundamental tone power for an input power between -25 dBm and -13 dBm.

The corresponding signal-to-noise-and-distortion ratio (SNDR) is plotted in Fig. 10. The maximum SNDR is achieved for an input power of -14 dBm, that is about 6 dB lower than $P_{\text{in},\text{dB}}$. It is 46 dB for a noise bandwidth of 4 MHz, 43 dB for a noise bandwidth of 20 MHz and 38 dB for a noise bandwidth of 60 MHz.

The adjacent-channel-leakage-power ratio (ACLR) for a UMTS-FDD downlink signal at 5 MHz and 10 MHz offset is 43 dB and 48 dB, respectively (Fig. 11), at an input power of -16.5 dBm. At an input power of -18 dBm, the ACLR is 46 dB and 47 dB at 5 MHz and 10 MHz offset, respectively. For an uplink signal, the ACLR at 5 MHz and 10 MHz offset is 49 dB and 51 dB, respectively, at an input power of -12 dBm. The corresponding output power is -10 dBm. The ACLR at 5 MHz offset is mainly limited by intermodulation, and the ACLR at 10 MHz offset is mainly limited by noise.

The measured composite EVM for a UMTS-FDD downlink signal is in the range from 14.3% at -30 dBm input power to 1.1% at -7.5 dBm input power (Fig. 12). This complies with the requirements for a base station using only QPSK modulation.

Figure 11. ACLR at -16.5 dBm input power/ -5.9 dBm peak envelope power.

Figure 12. EVM at -7.5 dBm input power/ +3.1 dBm peak envelope power.

IV. CONCLUSION

A fourth-order continuous-time bandpass delta-sigma modulator clocked at 7.5 GHz for a center frequency of 2.2 GHz is presented. The modulator has a multi-feedback architecture and uses low-noise series degenerated transconductors. It consumes 450 mW from a 3.6 V supply. It achieves a peak SNR of 45 dB and a peak SNDR of 43 dB in a bandwidth of 20 MHz. The UMTS-FDD ACLR for uplink transmission is 49 dB at 5 MHz offset and thus well beyond the requirements.

ACKNOWLEDGMENT

The authors thank Infineon for layout and tape-out support.

REFERENCES


