A 1.55 GHz to 2.45 GHz Center Frequency Continuous-Time Bandpass Delta-Sigma Modulator for Frequency Agile Transmitters

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Abstract—This paper presents a 4th order continuous-time bandpass delta-sigma modulator (CT-BPDSM) with a programmable center frequency ranging from 1.55 GHz to 2.45 GHz. The modulator is suited to be applied in multi-standard class-S power amplifiers. The circuit features a multi-feedback architecture with return-to-zero (RZ) and half-return-to-zero (HRZ) pulses. The loop filters consist of LC-resonators with emitter degenerated input transconductors and Q-enhancement circuits. A configuration register allows to program the resonator input transconductors, the Q-enhancement circuits and the resonator capacitances with 5 bit resolution. Fine tuning of the resonator center frequency is achieved with varactors. The circuit is implemented in a 200 GHz-fT SiGe-bipolar technology. The measured SNR at 2.2 GHz center frequency is 45.5 dB in a bandwidth of 20 MHz. At 1.55 GHz the SNR decreases to 40.7 dB. The measured uplink UMTS-FDD ACLR (adjacent channel leakage power ratio) of the modulator output is 48.4 dB in the first adjacent channel.

Index Terms — Delta-sigma modulator, class-S power amplifier, bipolar integrated circuit.

I. INTRODUCTION

The strong growth of mobile communications has led to many different standards. Users expect their mobile terminals to work in any environment and at different locations, whereas operators want to minimize their hardware effort by reconfigurable or programmable base station equipment. As a result, mobile terminals as well as base stations should provide access to several coexisting standards in different frequency bands.

The coding schemes in recent standards like UMTS (Universal Mobile Telecommunications System) exhibit higher peak to average power ratios (PAPR) than older ones like GSM (Global System for Mobile communications). This turns out to be a severe problem for the power amplifier (PA) in the transmission chain: The higher the PAPR the higher the back-off a conventional linear PA has to provide and thus the lower the power efficiency will be.

The multitude of coexisting standards and the PA power efficiency are two of the most important issues that suppliers of RF transmitters have to face in the next years. The class-S concept is seen as an attractive solution to both – power efficiency and multi-standard, multi-band operation [1, 2]. In a transmission chain with class-S concept the conventional linear PA is replaced by a power efficient switching-mode amplifier. The pulse sequence for the switching-mode amplifier input is generated from the analog RF-signal by a continuous-time bandpass delta-sigma modulator (CT-BPDSM). A bandpass filter reconstructs the analog signal at the output of the PA (Fig. 1). In the long term digital delta-sigma signal processing in CMOS [3, 4] with upsampling from base band to the switching-mode amplifier input is considered as both cost- and energy-efficient. However, the required clock frequency for signal frequencies above 2 GHz is not reached yet with current CMOS technologies. With a continuous-time BPDSM higher signal frequencies can be achieved due to fast analog signal processing. As an analog RF input signal is required, only the PA is replaced by the switching mode amplifier and the reconstruction filter in the transmission chain. This allows for upgrades of existing RF transmitters. As well, CT-BPDSMs remain the only solution for modulators in class-S amplifiers with signal frequencies well beyond 2 GHz in the near future.

The experimental results of a CT-BPDSM with a fixed center frequency at 2.2 GHz will be presented elsewhere [5]. This work describes a CT-BPDSM for multiband operation. The paper is organized as follows: In Section II the architecture of the modulator and the most important circuit blocks are described. Measurement results are presented in Section III and in Section IV a short conclusion is given.

II. CIRCUIT DESIGN

A. System architecture

Fig. 2 shows the block diagram of the circuit. A multi-feedback architecture with RZ and HRZ pulses is used for the modulator [6]. HRZ pulses are generated by a latch with a subsequent RZ latch. The feedback currents k_{1r}, k_{1h}, k_{2r} and k_{3h} can be controlled by externally applied currents via current mirrors.
The $G_q$ transconductors compensate for resistive losses in the resonator. The transconductors $G_m$ allow to control the resonator voltage swing. The transconductors are decoupled at the input by emitter followers. All transconductances and the capacitances in the resonators can be controlled separately via a configuration register with a resolution of 5 bit.

In order to prevent metastability of the clocked comparator a preamplifier is used. The preamplifier introduces additional excess loop delay. The loop delay is compensated by driving the comparator with a clock signal that is delayed versus the clock signal of the digital to analog converters (DAC). Layout caused parasitic effects that influence the excess loop delay are minimized by a signal flow oriented layout of the clock and the signal path.

**B. Programmable transconductance**

The lower end of the modulator dynamic range is governed by the noise currents that are injected into the resonators by the loss of the inductors, by the switchable capacitors and by the transconductors. The upper end of the dynamic range is limited by the transconductors’ nonlinearity. For a large dynamic range, low-noise transconductors with high linearity are needed. This can be achieved with emitter-degenerated differential pairs.

Fig. 3 shows two different topologies for the emitter degeneration. The transconductor in Fig. 3 (a) requires a higher supply voltage due to the series resistor. For this circuit only the higher pair transistors and degeneration resistors have a significant noise contribution. The noise of the common current source transistor and degeneration resistor appears as a common mode voltage at the differential output. The circuit in Fig. 3 (b) exhibits more circuit noise. The noise currents that are generated by the two current source transistors and current source degeneration resistors couple into the two complementary outputs separately. The current source noise is not converted to a common mode signal at the differential output. The difference in noise power at the differential outputs was simulated to be 4.6 dB, therefore the transconductor in Fig. 3 (a) is chosen for this design.

Each transconductor is set up of 5 binary weighted stages that can be switched on and off separately. Currents $I_{ctrl}$ from the configuration register control the bias voltage $V_b$ of the current source of the individual transconductors via the circuit in Fig. 3 (c) and thus allow the individual stages to be switched on and off.

**C. Programmable resonator capacitance**

The capacitance of the differential LC resonator consists of two fixed capacitors $C_{fix}$ connected to ground, five binary weighted capacitors $C_i$ with switches $s_i$ for coarse tuning and a varactor $C_{var}$ for fine tuning. Fig. 4 shows the circuit that implements a switchable differential capacitor $C_i$. It consists of two capacitors $C_i$ that are connected to the differential signal lines with one plate and to the emitters of switchable emitter followers with the other plate. If the emitter followers are switched on by $I_{ctrl}$, both capacitors are connected between one of the differential signals and a complementary signal replica that is generated by the emitter follower. For $I_{ctrl} = 0$ the capacitors are floating and the effective capacitance between the differential signal lines is minimized. The total effective capacitance $C_{eff}$ between the differential signal lines can be calculated as

$$C_{eff} = \frac{C_{fix}}{2} + \sum_{i=1}^{5} s_i C_i + C_{var} \quad \text{with} \quad s_i \in \{0,1\}.$$
III. EXPERIMENTAL RESULTS

The chip is implemented in a 200 GHz f_t SiGe bipolar technology (B7HF200) from Infineon and occupies a chip area of 2.2 mm². A chip photograph is shown in Fig. 5. The measurement setup consists of a Rohde&Schwarz SMF-100A for the generation of the clock signal, a SMU-200 for sinusoidal and modulated RF input signals and the spectrum analyzer FSQ-8. Measurements are automated with GPIB and read out with Matlab. 180°-hybrid directional couplers are used for single-ended-to-differential conversion for the clock and the input signal and for the differential-to-single-ended conversion of the output signal. The clock frequency is 7.5 GHz for all measurements.

The output spectrum for an input signal frequency of 2.2 GHz can be seen in Fig. 6. The measured single-ended output signal swing is 250 mV. The circuit draws 1.06 W from a 3.1 V supply including the bipolar configuration and control circuitry. Output signal and noise power in a bandwidth of 20 MHz are plotted in Fig. 7 versus the input power. The change from linear operation to compression is very abrupt. The modulator starts to get saturated for an input power about one dB below the 1-dB compression point. This is also exactly the point where the output power begins to deviate from its linear increase with the input power. Therefore a reasonable estimate for the peak SNR within the linear operation range is measured one dB below the 1-dB compression point. The noise power density is measured at 10 MHz offset from the carrier. The noise power is flat in a bandwidth of at least 25 MHz around the carrier (see also Fig. 9). The measured peak SNR is 45.5 dB in a bandwidth of 20 MHz.

The output signal and noise power is plotted versus the center frequency tuning range in Fig. 8. Output and noise power are measured at the point of the peak SNR described above. While the output power saturates at about the same power level for all frequencies, the noise power increases for lower signal frequencies. This is caused by the decreasing Q factor of the resonator for lower frequencies. However, the measured peak SNR at 1.55 GHz is still 40.7 dB. The dissipated power increases moderately from 992 mW at 2.45 GHz to 1.27 W at 1.55 GHz. This is due to the current that is consumed by the emitter followers in the switchable capacitors C_i.

The peak SNR of the modulator could be made even larger with a better Q factor of the resonators. Unfortunately the programmable Q-enhancement circuits are too weak to cancel all the resonator losses. This is due to an underestimation of the resonator losses in the design process and will be corrected in future designs.

One of the most important criteria for RF transmitters is the adjacent channel leakage power ratio (ACLR). The power ratio of modulated UMTS-FDD (frequency division duplex) uplink and downlink signals is measured (Fig. 9). For uplink transmission, the modulator reaches an ACLR of 48.4 dB and 49 dB for channels that are 5 MHz and 10 MHz offset from the carrier, respectively, at an input power level of -11dBm. For a UMTS-FDD downlink signal the measured ACLR is 42.8 dB at 5 MHz offset and 43.5 dB at 10 MHz offset at an input power level of -17 dBm.
Figure 8. Output power and corresponding noise power in a bandwidth of 20 MHz versus modulator center frequency measured at the point of the peak SNR as indicated in Fig. 7.

Figure 9. ACLR measurement for UMTS FDD downlink transmission. The signal is centered at 2.2 GHz, the adjacent channels at ±5 MHz and ±10 MHz are marked with a hatching pattern.

TABLE I. COMPARISON OF DELTA-SIGMA MODULATORS IN THE GHz FREQUENCY RANGE

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*normalized to a bandwidth of 1 MHz

A comparison of delta-sigma modulators in the GHz frequency range is given in Table I. This is the first tunable modulator that reaches signal frequencies beyond 2 GHz while using a moderate clock frequency of 7.5 GHz that is suited for switching mode RF power amplifiers.

CONCLUSION

A CT-BPDSM with a continuous center frequency tuning range of 900 MHz is presented for the first time. The large tuning range is based on configurable resonator capacitors that are implemented with switchable emitter followers. Moreover, input and Q-enhancement transconductors are configurable. The measured SNR in 20 MHz bandwidth is 45.5 dB at a signal frequency of 2.2 GHz while the modulator consumes 1.06 W from a 3.1 V power supply. The UMTS-FDD ACLR for uplink transmission is 48.4 dB and thus well beyond the requirements. The SNR and the ACLR can be further improved by extended Q-enhancement circuits.

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REFERENCES