Derivation of Single-Ended CMOS Inverter Ring Oscillator Close-In Phase Noise from Basic Circuit and Device Properties

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Abstract — A closed-form expression of close-in phase noise is derived for single-ended CMOS inverter ring oscillators. Close-in phase noise is expressed depending on the MOSFETs’ channel length $L_{\text{eff}}$, the oscillator stage number $n$, the NMOS and PMOS flicker noise coefficients $K_{F_N}$ and $K_{F_P}$ and the peak currents $I_{\text{DN}}$ and $I_{\text{DP}}$ that discharge and charge the node capacitances. Design implications regarding stage number $n$ and gate length $L$ are derived and verified by measurements. Further, the dependency of close-in phase noise on inverter symmetry is investigated. An optimum ratio of PMOS to NMOS channel width is derived and shown to be dependent on $K_{F_N}$ and $K_{F_P}$. The derived optimum ratio substantially deviates from the value for waveform symmetry. This characteristic is also confirmed by measurements.

I. INTRODUCTION

The noise spectrum of an electrical oscillator can be divided into three regions with the noise power shaped $\sim 1/\Delta f^3$, $\sim 1/\Delta f^2$ and a constant noise floor, respectively [1]. Close to the carrier, phase noise is dominated by upconverted $1/f$-noise and the noise power is shaped $\sim 1/\Delta f^3$. Due to the large $1/f$-noise of short-channel MOSFETs and the lack of passive resonant elements, CMOS ring oscillators tend to have a wide $1/\Delta f^3$-region.

This paper concentrates on deriving an expression of phase noise for this region and on achieving some design guidelines for CMOS inverter ring oscillators (fig.1).

II. CLOSE-IN PHASE NOISE THEORY

The basic idea is to regard close-in phase noise as a result of the low frequency fluctuations of the CMOS inverter propagation delays. The delay fluctuations again are caused by the fluctuations of the MOSFET drain currents (due to low-frequency noise), that charge and discharge the node capacitances.

The rise and fall times of CMOS inverter gates can be expressed as

\[
t_{\text{HL}} = \frac{C_{\text{node}}V_{\text{DD}}}{I_{\text{IN}}} \quad \text{and} \quad t_{\text{LH}} = \frac{C_{\text{node}}V_{\text{DD}}}{I_{\text{DP}}},
\]

where $I_{\text{DN}}$ and $I_{\text{DP}}$ are the average peaks (average referred to the time interval $t_{\text{IN}}$ or $t_{\text{LH}}$) of the NMOS and PMOS drain currents $i_{\text{DN}}$ and $i_{\text{DP}}$ that discharge and charge the node capacitance $C_{\text{node}}$, respectively. A rough estimate of the propagation delays for falling and rising edges is [2]

\[
t_{\text{PHL}} = \frac{1}{2}t_{\text{PHL}}, \quad t_{\text{PHL}} = \frac{1}{2}t_{\text{LH}}.
\]

The cycle time $T$ of a CMOS inverter ring oscillator with $n$ stages is the sum of all falling- and rising-edge propagation delays:

\[
T = \sum_{i=1}^{n} (t_{\text{PHL}} + t_{\text{PHL}}).
\]

Now, the effect of low frequency current noise on the phase deviation $\phi(t)$ shall be examined in the time-domain. Low frequency MOSFET drain current noise can be seen as a low frequency modulation of the average peak drain currents $i_{\text{DN}}(t)$ and $i_{\text{DP}}(t)$:

\[
i_{\text{DN,P}}(t) = i_{\text{DN,P}}(t) + n_{\text{IN,P}}(t),
\]

The current $i_{\text{DN,P}}$ represents the nominal average peak current of the NMOS or PMOS and $n_{\text{IN,P}}(t)$ represents the normalized, time-dependent deviation from the nominal value in stage $i$ due to low-frequency current noise.

Following (1), (2), (4) and using the relation $1/(1+x) \approx 1-x$ for $x \ll 1$, the time-dependent “noisy” propagation delay is

\[
t_{\text{PHL}}(t) = \frac{C_{\text{node}}V_{\text{DD}}}{2I_{\text{DN}}} (1 - n_{\text{IN}}(t)) = t_{\text{PHL}} (1 - n_{\text{IN}}(t)).
\]

The delay $t_{\text{PL}}$ can be expressed accordingly using $i_{\text{IN}}(t)$ and $n_{\text{IN}}(t)$. The time-dependent cycle time reads

\[
T(t) = \sum_{i=1}^{n} (t_{\text{PHL}} (1 - n_{\text{IN}}(t)) + t_{\text{PHL}} (1 - n_{\text{IN}}(t))).
\]

The cycle time $T(t)$ can be decomposed into a nominal value $T_0$ and a time dependent varying value $\Delta T_{\text{cycle}}(t)$:

\[
T(t) = T_0 + \Delta T_{\text{cycle}}(t),
\]
With (11), the corresponding phase deviation is
\[
\Delta T_{\text{cycle}}(t) = \sum_{n=1}^{N} \left( t_{\text{phL}} + t_{\text{phH}} \right) = n \left( t_{\text{phL}} + t_{\text{phH}} \right) = 2n \tau_f.
\]  
(8)

The time-dependent deviation of the zero-crossing time of a certain oscillator signal from its nominal value is
\[
\Delta T_{\text{zc}}(t) = \sum_{n=1}^{N} \Delta T_{\text{cycle}}(\tau) \sim \int_{0}^{T_0} \frac{\Delta T_{\text{cycle}}(\tau)}{T_0} d\tau.
\]  
(10)

The corresponding phase deviation is given by
\[
\phi(t) = 2\pi \frac{\Delta T_{\text{zc}}(t)}{T_0} = 2\pi \int_{0}^{t} \frac{\Delta T_{\text{cycle}}(\tau)}{T_0} d\tau
\]
\[= -2\pi \frac{1}{2} \sum_{n=1}^{N} \left( t_{\text{phL}n} \sin(\omega_n t) + t_{\text{phH}n} \sin(\omega_n t) \right) d\tau.
\]  
(11)

To deduce an expression of phase noise, an oscillator with only one noisy NMOS in a certain stage shall be considered. To simplify the calculations, the power density spectrum of the normalized low-frequency drain current noise is at first assumed to have to discrete lines at \( \pm f_{\text{m}} \):
\[
n_{\text{in}}^2(\Delta f) = n_{\text{in}}^2 \delta(\Delta f - f_{\text{m}}) + \delta(\Delta f + f_{\text{m}}).
\]  
(12)

The according time-domain normalized noise current is
\[
n_{\text{in}}(t) = 2n_{\text{in}} \cos(\omega_{\text{n}} t).
\]  
(13)

With (11), the corresponding phase deviation is
\[
\phi(t) = -\frac{2\pi}{2} \sum_{n=1}^{N} n_{\text{in}}(t) \sin(\omega_{\text{n}} t) \approx \phi_{\text{m}} \sin(\omega_{\text{n}} t).
\]  
(14)

The single-sideband phase noise \( \phi_{\text{m}}(f_{\text{m}}) \) of a signal with phase \( \phi(t) = \phi_{\text{m}} \sin(\omega_{\text{n}} t) \) was shown to be equal to \( \phi_{\text{m}}/4 [3] \). Therefore, the normalized NMOS drain current noise with a continuous power spectral density \( n_{\text{in}}^2(\Delta f) \) causes single-sideband phase noise given by
\[
\phi_{\text{m}}^2(\Delta f) = \frac{\phi_{\text{m}}^2}{4} = \frac{\phi_{\text{m}}^2}{4} \frac{\Delta f}{\Delta f_{\text{m}}} n_{\text{in}}^2(\Delta f) = \frac{f_{\text{m}}^2}{4} \tau_f \frac{\Delta f}{\Delta f_{\text{m}}} n_{\text{in}}^2(\Delta f).
\]  
(15)

With (8), (15) and all n NMOS and PMOS noise powers added, \( \phi_{\text{m}}^2(\Delta f) \) is given by
\[
\phi_{\text{m}}^2(\Delta f) = \frac{f_{\text{m}}^2}{4} \Delta f \left( n_{\text{in}}^2(\Delta f) + n_{\text{phL}}^2(\Delta f) + n_{\text{phH}}^2(\Delta f) \right).
\]  
(16)

Now, (16) shall be transformed to a shape where the influence of the average peak currents is observable. The propagation delays \( t_{\text{phL}} \) and \( t_{\text{phH}} \) can be resubstituted:
\[
t_{\text{phL}} = \frac{C_{\text{in}} V_{\text{DD}}}{2 I_{\text{DN}}}, \quad t_{\text{phH}} = \frac{C_{\text{in}} V_{\text{DD}}}{2 I_{\text{DP}}},
\]  
(17)

\[
\tau_f = \frac{f_{\text{m}}^2}{4} \left( t_{\text{phL}} + t_{\text{phH}} \right) = \frac{C_{\text{in}} V_{\text{DD}}}{2 I_{\text{D}}},
\]  
(18)

The value \( \tau_{\text{D}} \) is equal to the DC-current consumption \( I_{\text{DC}} \), that is governed by the periodic charging of \( n C_{\text{node}} \):
\[
\tau_{\text{D}} = \frac{2 f_{\text{DN}} - 1}{4 \tau_f} = \frac{C_{\text{node}} V_{\text{DD}}}{2 I_{\text{D}}}, \quad n_{\text{node}} = \frac{V_{\text{DD}}}{I_{\text{D}} - 2 I_{\text{DN}}}, \quad I_{\text{DC}} = I_{\text{D}}.
\]  
(19)

The drain current 1/f noise spectral density \( S_{\text{in}}(\Delta f) \) of a DC-biased MOSFET can be modeled as follows [4]:
\[
S_{\text{in}}(\Delta f) = \frac{\Delta f}{f_{\text{in}}} \frac{\Delta f}{f_{\text{in}}} \frac{\Delta f}{f_{\text{in}}} C_{\text{ox}} \frac{L_{\text{eff}}}{1 + \frac{V_{\text{DD}}}{V_{\text{DD}}}}
\]  
(20)

Usually, \( \text{EF} = \text{AF} = 1 \) holds and \( K \) is a technology dependent parameter. The normalized power spectral density \( n_{\text{in}}(\Delta f) \) relates \( S_{\text{in}}(\Delta f) \) to \( I_{\text{in}}^2 \):
\[
n_{\text{in}}^2(\Delta f) = \frac{1}{I_{\text{D}}} \frac{K}{\Delta f} \frac{C_{\text{ox}}}{I_{\text{D}}} \frac{L_{\text{eff}}}{1 + \frac{V_{\text{DD}}}{V_{\text{DD}}}}.
\]  
(21)

As the currents \( i_{\text{in}}(t) \) and \( i_{\text{ph}}(t) \) in the oscillator can be approximated as square waves, their normalized power spectral density \( n_{\text{in}}(\Delta f) \) is equal to the DC-case for \( \Delta f \ll f_{\text{in}} \). Thus, \( I_{\text{in}}^2 \) can be replaced by \( I_{\text{D}} \). With (17) to (21) and \( L_{\text{cen}} = L_{\text{cen}} = L_{\text{cen}} \) (16) reads:
\[
\phi_{\text{m}}^2(\Delta f) = \frac{f_{\text{m}}^2}{4} \frac{2 n I_{\text{in}}^2}{n I_{\text{in}}^2} \frac{I_{\text{in}}^2}{I_{\text{D}}} \frac{1}{I_{\text{D}}} \frac{K}{\Delta f} \frac{C_{\text{ox}}}{I_{\text{D}}} \frac{L_{\text{eff}}}{1 + \frac{V_{\text{DD}}}{V_{\text{DD}}}}
\]  
(22)

To do a fair comparison of oscillators with different \( I_{\text{DC}} \) and \( f_{\text{in}} \) a normalized phase noise value (also called figure of merit) \( \phi_{\text{m}}(\Delta f) \) can be calculated and decomposed into four multipliers \( I_{\text{m}} \) to \( I_{\text{m}} \):
\[
\phi_{\text{m}}(\Delta f) = \frac{f_{\text{m}}^2}{4} \frac{2 n I_{\text{in}}^2}{n I_{\text{in}}^2} \frac{I_{\text{in}}^2}{I_{\text{D}}} \frac{1}{I_{\text{D}}} \frac{K}{\Delta f} \frac{C_{\text{ox}}}{I_{\text{D}}} \frac{L_{\text{eff}}}{1 + \frac{V_{\text{DD}}}{V_{\text{DD}}}}
\]  
(23)

The smaller \( \phi_{\text{m}}^2(\Delta f) \), the better the oscillator. Multiplier \( I_{\text{m}} \) and thus \( \phi_{\text{m}}^2 \) is still a function of frequency offset \( \Delta f \), it has a -10dB/decade slope. This is important to keep in mind when comparing oscillators in the 1/\( \Delta f \)-region.

III. DESIGN IMPLICATIONS

The second multiplier \( I_{\text{m}} \) in (23) is usually given by the technology. Only the multipliers \( I_{\text{m}} \) and \( I_{\text{m}} \) can be optimized by the circuit designer. \( M_{\text{m}} \) is determined by stage number \( n \) and gate length \( L_{\text{cen}} \). \( M_{\text{m}} \) gives a hint on the dimensioning of the NMOS and PMOS peak currents.
A. Enlargement of C_{node}, n or L_{eff}

The following considerations are starting from an oscillator with a high oscillation frequency f_0. It has a small stage number n_0 and comprises MOSFETs with minimum gate length L_{min}. Moreover, the inverters are symmetric, i.e. W_N = \mu_p/\mu_N W_N. The design goal is to implement a oscillator with a lower oscillation frequency f_0. It has a symmetric inverter, even if the trap densities of the PMOS and NMOS channel width. Thus, with KF \sim \mu_N [4], the optimum W_p/W_N ratio is

\[
\frac{W_p}{W_N} = \frac{\mu_N KF}{\mu_p KF} = \frac{\mu_N}{\mu_p} \frac{N_{effP}}{N_{effN}}.
\] (36)

N_{effP} is the effective oxide trap density in the NMOS and PMOS transistor, respectively.

B. Influence of PMOS to NMOS gate width ratio W_p/W_N

The multiplier M_4 in equation (23) can be transformed to reveal the influence of PMOS and NMOS channel width. With the average peak drain current I_D, proportional to gate width W and carrier mobility \mu, the following values can be defined:

\[
\bar{\mu}W = 2\left(\mu_N W_N\right)^{-1} + \left(\mu_p W_p\right)^{-1},
\] (30)

\[
w_{effN} = \frac{\mu_N W_N}{\bar{\mu}W}, \quad n_{effP} = \frac{\mu_p W_p}{\bar{\mu}W}.
\] (31)

With w_{effP} = 2 \cdot w_{effN}, the multiplier M_4 of (23) reads:

\[
\mathcal{E}_{norm}(\Delta f) = K \left[ \left(1/w_{effN}\right)^3 KF_N + \left(2 - 1/w_{effN}\right)^3 KF_P \right].
\] (32)

To find the minimum, \mathcal{E}_{norm} is differentiated:

\[
\frac{\partial \mathcal{E}_{norm}}{\partial \left(1/w_{effN}\right)} = K \left[ 3 - \left(1/w_{effN}\right)^2 \right] KF_N - 3 \left(1/w_{effN}\right)^2 KF_P.
\] (34)

The minimum \mathcal{E}_{norm}-value is obtained for

\[
\frac{w_{effN}}{w_{effP}} = \frac{\mu_p W_p}{\mu_N W_N} = \sqrt{\frac{KF_P}{KF_N}}.
\] (35)

Thus, with KF \sim \mu_N [4], the optimum W_p/W_N ratio is

\[
\frac{W_p}{W_N} = \sqrt{\frac{KF_P}{KF_N}} = \sqrt{\frac{\mu_N}{\mu_p} \frac{N_{effP}}{N_{effN}}}.
\] (36)

N_{effP} is the effective oxide trap density in the NMOS and PMOS transistor, respectively.

In [5], waveform symmetry is said to lower the upconversion of device 1/f-noise to phase noise. But the value (W_p/W_N)_{sym} for waveform symmetry (i.e. \tau_{sym} = \tau_{opt}), approximately given by

\[
\frac{W_p}{W_N} = \frac{\mu_N}{\mu_p},
\] (37)

substantially deviates from the value (W_p/W_N)_{opt} derived here. W_p has to be decreased in comparison to the symmetric inverter, even if the trap densities of the PMOS and NMOS transistors are equal. If N_{effP} < N_{effN}, as observed in [4], W_p has to be decreased further. A commonsense explanation is as follows: If the PMOS has lower 1/f-noise than the NMOS, it’s contribution to the cycle time T_0 has to be increased. Thus \tau_{sym} should be larger than the more "noisy" \tau_{opt}, and W_p has to be decreased.
III. MEASUREMENT RESULTS

A. Oscillators according to strategy C, N, WL

Figure 2. Measured £ against Δf with 1/Δf²-trend lines

The three oscillators with symmetrical inverters were realized in 0.18 µm standard CMOS technology. Figure 2 shows the measured phase noise and Table 1 summarizes the results. Compared to the C-oscillator, £norm is 5 dB lower for the N-oscillator with tripled number of stages. The improvement expected by theory is 10 log(3) = 4.8 dB. £norm is 8 dB lower for the oscillator with doubled channel length. The expected value is 10 log(2) = 6.0 dB for $C_C < C_P$. As $L_{in} < L$, the expected value is probably underestimated.

Table 1. Ring oscillator C, N and WL measurement results.

| osc. | L_{min} | n  | V_m{|V|} | I_m{|mA|} | f_{m}{[GHz]} | £^{**} | £_{norm}^{**} |
|------|--------|----|--------|---------|-------------|---------|-------------|
| C    | 1 3    | 1.82 | 3.87   | 2.50    | -83.1       | -148.7  |
| N    | 2 9    | 1.84 | 3.87   | 2.15    | -90.0       | -154.1  |
| WL   | 2 3    | 1.84 | 3.56   | 2.25    | -92.1       | -156.9  |

B. Oscillators with different gate width ratio $W_p/W_n$

Two oscillators with different $W_p/W_n$ ratio were processed by different manufacturers, but both using 0.18 µm standard CMOS technology. To detect possible differences in the device 1/f-performance of the two technologies, the £norm-values of quadrature ring oscillators (Q-oscillators, [6]) - realized in both technologies with the same device dimensions - were compared. Table 2 summarizes the results. The Q-oscillator processed by supplier A performs 1 dB better than the one processed by B. The £norm-value of the N-oscillator with severe unsymmetrical inverters ($W_p/W_n = 0.4$, supplier B) is equal to the £norm-value of the N-oscillator with symmetrical inverters ($W_p/W_n = μ_{CP}/μ_{NP} = 2.7$, supplier A), even though the stage number is smaller and supplier A seems to perform slightly better. Accordingly, the optimum ratio ($W_p/W_n$)opt should be somewhere in between 0.4 and 2.7. This result confirms that waveform symmetry is not the optimum for CMOS inverter ring oscillator phase noise performance and that the PMOS portion of the total delay must be larger than the NMOS portion. The noise advantage of PMOS transistors in ring oscillators coincides with measurements of LC-oscillators [7].

Table 2. Comparison of ring and quadrature oscillators

<table>
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<th>W_{n}{[mA]}</th>
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V. CONCLUSION

Single-ended CMOS inverter ring oscillator close-in phase noise performance can be optimized either by enlarging the stage number or, even better, by enlarging the channel length. The normalized phase noise was measured to be 5 dB lower for an oscillator with tripled number of stages and 8 dB lower for an oscillator with doubled gate length compared to an oscillator that has enlarged node capacitors. The optimum gate width ratio $W_p/W_n$ is shown to be determined by the flicker noise coefficients KF_N and KF_P. As KF_P usually is lower than KF_N, the PMOS width has to be decreased compared to a symmetrical CMOS inverter design.

REFERENCES