Integrator and Digitizer for a non-coherent IR-UWB Receiver

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Abstract—Impulse-radio ultra-wideband systems (IR-UWB) provide short-range wireless communication and precise localization simultaneously. Especially non-coherent IR-UWB reduces the system complexity which enables the design of low-power receivers. This paper presents an integrating digitizer which integrates rectified baseband pulses of an IR-UWB signal and provides the digitized data to the digital baseband of the receiver.

The integrator is composed of two time-interleaved (TI) operational amplifiers with capacitive feedback. With this structure, the integrator can be periodically reset without introducing a dead time between two integration periods. The analog-to-digital conversion is performed by a 6 bit 62.4 MS/s successive approximation register analog-to-digital converter (SAR ADC). The integrating digitizer chip is realized in a 250 nm SiGe:C BiCMOS technology from IHP.

I. INTRODUCTION

Presently UWB systems are the first choice for short-range medium data rate wireless communication and localization systems. They can coexist with other wireless systems because the transmitted power spectral density is low enough not to disturb narrow-band signals. In IR-UWB systems, the available bandwidth is covered by a single channel. In time-domain, this wideband signal consists of short pulses. Applying non-coherent detection, only the energy and not the phase of the received signal is evaluated. This relaxes the requirements of the A/D conversion and lowers the circuit complexity which is advantageous for a low-power design.

Formerly published non-coherent IR-UWB receivers are implemented with a passive [1] or active [2] low pass filter instead of an integrator and no ADC is included. Another realization [3] utilizes an operational amplifier (op-amp) based RC integrator followed by an ADC that dissipates a large amount of power which is not suitable for low-power operation. The integration of the output current of the rectifier onto a capacitor has been shown [4]. This capacitor holds the signal for the A/D conversion and is reset before the subsequent integration period. But this approach introduces a dead time during the hold and the precharge phases.

The proposed circuit is designed for a fully integrated IR-UWB transceiver SoC according to the standard IEEE 802.15.4a for communication with a data rate of 850 kbit/s and localization with accuracy in the range of centimeters. The topology of the integrator allows operation without a dead time which avoids the loss of received pulses. The A/D-conversion is performed by a SAR ADC.

This paper is organized as follows: Section II explains the system setup and implementation. Simulation and measurement results are given in Section III and Section IV concludes the paper.

II. IMPLEMENTATION

The intended IR-UWB receiver operates according to the standard IEEE 802.15.4a. The received signal is converted to the baseband and rectified prior to the integrating digitizer. The resulting sequence of positive pulses is applied to the integrator. A SAR ADC converts the integrated signal to the digital domain and provides the data to the digital baseband processor. The block diagram is shown in Fig. 1. A 499.2 MHz clock is applied and ensures synchronicity of the integrator and the ADC. The input signal \( V_{in} \) is distributed to both integration paths. The digital output code \( D_5 \) (most significant bit, MSB) to \( D_0 \) (least significant bit, LSB) is provided to the digital baseband processor. The integration relaxes the required ADC sampling rate to 62.4 MS/s which also decreases the required computational speed of the digital baseband processor and thus saves power.

The integration of mixed signal components into one chip demands careful design because digital switching may distort analog signals. In order to mitigate these effects, this circuit employs fully differential signaling. It is implemented in the 250nm SiGe:C BiCMOS technology SGB25V from IHP.
The integrator detects the received energy within one integration period of 16 ns. This corresponds to the duration of eight pulses. In order to provide an integration without a dead time the integrator is designed as a twofold time-interleaved circuit as shown in Fig. 1. The input is distributed to two integrator cores (Fig. 2) composed of op-amps with capacitive feedback and resistive inputs [5] that are activated alternately. The control signals are generated by logic combinations of divided clock signals. At the end of the integration period, the output signal remains constant and a 2:1 multiplexer forwards it to the ADC.

Fig. 3 shows the timing diagram of the two integrator cores Int1 and Int2. At \( t_0 \), Int1 has been reset and starts integrating. After 16 ns, the integration period is stopped by disconnecting the inputs. The voltage is held for 8 ns which suffices the ADC for sampling. Int1 is reset during the next 8 ns by shortcutting the integration capacitors. For Int2, the same sequence of operation modes is shifted by 16 ns. The analog MUX is a p-channel MOSFET switch and forwards the hold and reset phases to the ADC.

B. Successive approximation analog-to-digital converter

The successive approximation principle is applied because it is suitable for low-power operation. A resolution of 4 bit meets the demands of the IR-UWB receiver [6]. However, due to the non-coherent receiver implementation, only positive voltages appear at the ADC input. Thus half of the voltage range is omitted and the required resolution increases by 1 bit. In order to exceed the minimum requirement a 6 bit SAR ADC is realized [7].

The SAR ADC and the TI integrator share the same 499.2 MHz system clock which guarantees synchronicity.

The ADC takes eight clock cycles for one conversion resulting in a conversion rate of 62.4 MS/s. The sampling period is 2 ns which is short enough to complete sampling during the hold phase of the TI integrator.

The SAR ADC requires three reference voltages that are generated on-chip. The reference voltages and the differential input voltages are amplified by emitter followers that are able to drive the input capacitance of the ADC.

Fig. 4 shows the layout and a photograph of the circuit occupying 1.4 \( \times \) 0.6 mm\(^2\). The integrator has an area of 90 \( \times \) 210 \( \mu \)m\(^2\) and the analog-to-digital converter 360 \( \times \) 280 \( \mu \)m\(^2\).

III. SIMULATION AND MEASUREMENT

A. Integrator

Simulations and measurements for a single TI integrator, a single analog-to-digital converter and the combination of both are presented. The integrating digitizer
An integrating digitizer for an IR-UWB receiver according to the standard IEEE 802.15.4a is presented. The time-interleaved structure of the integrator prevents a dead time.

Measurement results show that the requirements of the IR-UWB receiver are fulfilled. The integrator has a linear transfer characteristic and the effective resolution of the ADC exceeds 5 bit up to Nyquist frequency. The number of on-pulses in an on-off-keyed pulse sequence can be determined reliably.

The integrator reduces the pulse rate of 499.2 Mpulses/s to a symbol rate of 62.4 Msymbol/s and relaxes the desired SAR ADC conversion rate to 62.4 Ms/s. The core components integrator, analog MUX and SAR ADC dissipate 16.15 mA from a 2.6 V supply.

REFERENCES


