High-Speed Comparators for SAR ADCs in 130 nm BiCMOS

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Abstract — This paper presents high-speed low-power
differential comparators in 130 nm SiGe BiCMOS technol-
ogy. The high sensitivity of 1.25 mV at 1 GHz clock fre-
quency is suited for high-speed high-resolution SAR analog-
to-digital converters. Power consumption is in the range
from 250 µW to 840 µW with a 1.2 V supply voltage. The
decision is taken by a regenerative latch with cross coupled
transistors. Four versions of the comparator are imple-
mented where different latch types are used: One latch with
p-channel MOS transistors, one with n-channel MOS transis-
tors and two ones with npn transistors. Measurements of the
bit error rate and the dead time as well as eye diagrams are
presented.

Index Terms — Analog-Digital Conversion, BiCMOS In-
tegrated Circuits, Comparators.

I. INTRODUCTION

Differential comparators compare a differential analog
input voltage with zero at the positive or the negative edge
of a clock signal [1], [2]. They translate small input sig-
als to CMOS or CML levels. This function is needed in
circuits like analog-to-digital converters.

The comparators which are proposed in this work are
designed for use in a successive approximation (SAR)
analog-to-digital converter [3]. Fig. 1 shows a block dia-
gram of a SAR analog-to-digital converter. The conver-
sion process is performed with a binary tree search. The
comparator decides which branches are to be taken.

High speed and high sensitivity as well as low power
consumption are crucial for this purpose. The comparator
speed directly influences the maximum sampling rate of
the analog-to-digital converter while sensitivity limits its
resolution.

For the design of analog-to-digital converters certain re-
quirements have to be met. The proposed comparators can
be scaled for a given resolution, sampling frequency or
power consumption.

As shown in Fig. 2 SAR analog-to-digital converters are
suitable for high parallelization [4]. Hence the power
consumption of core components has to be minimized.
Thus low power comparators are a key issue.

High-speed low-power operation makes the compar-
ators suitable for wireless systems as well. In ultra wide
band applications input signals with very low amplitudes
are processed. The high sensitivity of the comparators
supports wireless system design.

The second section describes the topology and function-
ality of the circuits. Measurement setup and results are
given in the third section. The fourth section concludes the
paper.

II. CIRCUIT DESIGN

Four comparator circuits are implemented in a 130 nm
SiGe BiCMOS technology. They work with a supply
voltage of 1.2 V. Inputs and outputs are designed for use
in a 50 Ω measurement environment.

The schematics of the comparators are shown in Fig. 3.
Each comparator has a reset phase Φ = 1 and a decision
phase Φ = 0.

During the reset phase MOS switch N0 (P0) is turned
off. Furthermore switches P3, P4 (N3, N4) reset the deci-
sion nodes to ground potential. No power is consumed
during reset as there is no current path from the supply to
ground.
During the decision phase the sign of the different input voltage at the gates of N1 and N2 (P1 and P2) is determined. A regenerative latch (P5 and P6 in Fig. 3a, N5 and N6 in Fig. 3b) amplifies the drain current difference of the input transistors (N1 and N2 in Fig. 3a, P1 and P2 in Fig. 3b, c and d). Static CMOS inverters ensure CMOS levels at the outputs. The circuit configuration with output drivers is shown in Fig. 4. Identical inverter chains are used for all circuits. This enables comparison of the different comparator cores.

All MOSFETs in circuit (b) are designed to have the same transconductance parameters $\beta$ like the corresponding ones in circuit (a). All MOSFETs in circuits (b) and (c) are equally sized. Transistors N5 and N6 are replaced by npn transistors Q5 and Q6 in circuit (c). Circuit (d) is a second variant of (c). P0 to P2 as well as N3 and N4 have enlarged channel widths so that the maximum allowed collector current is applied to Q5 and Q6 during the decision phase.

Circuit (a) uses n-channel input transistors. This leads to small input devices and therefore small input capacitance. It uses a negative supply voltage that can be switched on or off by n-channel transistor N0.

In (b), all n-type transistors are replaced by p-type ones and vice versa. The supply voltage is positive and can be switched by P0.

In (c), the n-channel latch is replaced by a latch with npn-type SiGe bipolar transistors. These bipolar transistors have a transit frequency $f_T = 250$ GHz which leads to fast operation of the comparator. The voltage level at the decision nodes is limited to the maximum base emitter voltage $V_{BE}$ of the bipolar transistors. This voltage is converted to static CMOS levels by inverters.

The device topology of circuit (d) is the same like (c). All MOSFETs have enlarged channel widths to allow the maximum collector current of Q5 and Q6 to flow during the decision phase. Furthermore larger devices and currents provide for a larger signal to noise ratio which causes the sensitivity to rise.

III. MEASUREMENT

A. Measurement Setup

Fig. 5 shows the measurement setup. A pseudo random bit sequence (PRBS) of variable amplitude and length $2^{31} - 1$ is applied to the input of the comparator. A correction of the offset voltage at the input is enabled by bias tees and a DC current source. The amplitude of the differential input signal is in the range of $1.25 \text{ mV} \leq V_{in} \leq 10 \text{ mV}$.

A 1 GHz clock signal with a duty cycle of 50 % is used. The clock divides the comparator operation into reset and decision phases of equal lengths. The input clock phase
can be adjusted to shift the sampling time.

The output signals of the comparator are analyzed with a sampling oscilloscope and with a bit error detector. The timing of the reset and decision process is investigated by eye diagram measurements of the output signals (Fig. 6).

Furthermore the dependence of the bit error rate on the differential input voltage amplitude is determined. This is a measure for the sensitivity of the comparator. For SAR analog-to-digital converters bit error rates in the range of $10^{-6}$ can be tolerated because an error usually causes a 1 LSB deviation only.

The dead time of the comparator circuits is determined by shifting the clock phase. Setting the sampling time to the edge of the input signal leads to invalid comparator decisions. A shift to the left or right of the edge causes the bit error rate to decrease. The points of time where the bit error rate drops below $10^{-6}$ are determined. The time difference between both points is the dead time of the comparator. The dead time does not only depend on the comparator itself but also on the quality of the input signal that is provided by a pulse pattern generator.

The circuits’ offset voltages are statistically examined. Input related offset voltages are determined for 20 samples of each circuit.

B. Measurement Results

Fig. 6 shows an exemplary eye diagram of circuit (b). A differential input voltage amplitude of $V_{iD} = 1.25$ mV is applied for this measurement. One whole comparator cycle with a reset phase and a decision phase is shown.

The graph is divided into two phases of equal length by two vertical bars. The clock signal is high during the reset phase, denoted as I. Both outputs are reset to ground and are forced to rest there during interval 1. The decision phase, denoted as II, starts when the clock signal changes from high to low. This point of time is indicated by the right bar.

Interval 2 begins at the right bar. It shows the decision time of the comparator. The decision nodes are charged by the drain currents of the input transistors P1 and P2 until the threshold voltage of one of the n-channel transistors N5 or N6 is reached. Then the regenerative latch that is formed by N5 and N6 amplifies the input signal exponentially.

In case of a differential input voltage amplitude of 1.25 mV the decision time is 230 ps for circuit (b). The decision time falls with rising input voltage amplitude because the difference of the input transistors’ drain currents rises. Therefore one decision node is charged faster and the threshold voltage is reached earlier.

The eye width is denoted by interval 3. For circuit (b) the eye is opened for 250 ps if a differential input voltage amplitude of 1.25 mV is applied. The eye width increases with rising input voltage amplitude.

Power consumption was derived by simulation and proven by measurement. The whole test circuit consumes about 30 mW at a 1.2 V power supply which is mainly caused by clock and output drivers. The comparator core power consumption depends on the circuit type and is 250 µW for circuits (a), (b) and (c) and 840 µW for circuit (d).

Fig. 7 shows the bit error rate (BER) of each circuit type over the input voltage amplitude. The sampling time is adjusted to achieve optimal results and the offset is compensated by a bias current $I_{\text{Offset}}$. The graph shows similar performance of circuits (a), (b) and (c) while circuit (d) shows a significantly smaller bit error rate. The reason for that is the increased signal-to-noise ratio due to larger devices and currents.

The advantage of circuit (c) over circuits (a) and (b) is its faster operation. Having the same power consumption, bit error rate and input capacitance the npn transistors enable a significant reduction of the decision time. For circuit (c), the decision time is reduced by 39 % compared to circuit (b). The decision time can further be reduced by increasing the MOSFETs’ channel widths and device currents as shown in circuit (d). Its decision time is re-
duced by 68% in comparison with circuit (b). As the delay time of a decision directly influences the maximum conversion rate of a SAR analog-to-digital converter, especially circuits (c) and (d) are suited for this purpose.

The decision time of circuit (a) is 370 ps which is much more than the other circuits. This is caused by the charging process of the decision nodes. Both node voltages cross the decision threshold of the CMOS inverters. Therefore both output signals change their values. The decision process is not completed before one output goes back to its initial value.

The comparators’ dead times are plotted in Fig. 8. All circuits (a) to (c) show similar performance. The reason for that are the input devices which are dimensioned for equal transconductance parameters and therefore have similar noise power.

Comparator (d) has a significantly shorter dead time. For a differential input voltage amplitude of 10 mV it is as low as 31 ps which is an improvement of 20 ps compared to the other circuits.

The measured standard deviations of the input related offset voltages are 2.9 mV, 4.1 mV, 4.6 mV and 1.9 mV for circuits (a), (b), (c) and (d), respectively.

The measurement results are summarized in Table 1.

### IV. CONCLUSION

Four high-speed low-power comparators are presented. They achieve high sensitivity and a low bit error rate at a sampling frequency of 1 GHz. The circuits are designed for use in a SAR analog-to-digital converter.

Their short dead time indicates a short setup time. Using a latch with npn transistors makes the decision very fast. This leads to a short delay time of the comparator which enables the SAR analog-to-digital converter to operate at high conversion rates.

For a BER < 10^{-6} the sensitivity is 2 mV for circuits (a) to (c) and 1.25 mV for circuit (d). If 1/2 LSB is equal to the input voltage amplitude for BER < 10^{-6} and if the differential analog input voltage range is ±1.25 V this corresponds to a resolution of 9 bit for circuits (a) to (c) and 10 bit for circuit (d).

The input related offset voltage is much larger than the sensitivity. Thus the offset voltage limits the resolution of a SAR-ADC-system with multiple analog-to-digital converters. But this problem can be solved by offset correction as shown in [5].

Furthermore the power consumption of the comparator cores lies between 250 µW and 840 µW. This allows to use them in massively parallelized SAR analog-to-digital converters.

### REFERENCES


