A 1.6 GHz Switch Mode Power Amplifier with Continuous-Time Bandpass Delta-Sigma Modulator

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Abstract
A continuous-time bandpass delta-sigma modulator (CT BDSM) is designed and fabricated in a SiGe bipolar transistor technology with a transit frequency of 200 GHz. The modulator can be tuned in its center frequency from 1.55 GHz up to 2.45 GHz for mobile base station applications. To drive a GaN high power amplifier a driver amplifier is presented using a complementary bipolar transistor technology.

I. INTRODUCTION
The worldwide success of mobile communication generates a great demand for power amplifiers at microwave frequencies. About half of power consumption of a base station is contributed by the power amplifier, therefore a high efficiency is required. The modulation schemes of the standards have changed from constant envelope signals to complex modulated signals with a large peak-to-average ratio of about 10 dB. Therefore, the efficiency of the power amplifier (PA) has not only to be high at the peak output power, but also at lower power levels even at 10 dB back-off [1].

Switching amplifiers are attractive for this application as they exhibit a theoretical limit of 100 % efficiency at all input power levels [2]. Real amplifiers show significant switching and dynamic losses due to the capacitance of the output node. As switching amplifiers only preserve the phase information by the zero crossings the radio frequency (RF) signal can not be amplified directly without first encoding of the RF signal into a binary amplitude pulse train for subsequent amplification. Several approaches are presented in the literature namely envelope elimination and restoration (EER) [3] and linearization with non-linear components (LINC) [4].

II. MODULATOR
The block diagram of the CT BPDSM is shown in fig. 2.
The continuous-time filters are monolithic integrated LC resonators. To compensate the losses of the resonator a transconductance $G_q$ is used for each stage. The transconductance $G_m$ in the signal path can be used to control the resonator voltage swing. The output signal of the second stage is amplified and stored in latches. The multi-feedback path is separated for each stage into the branches for the two halves of the clock period improving the noise shaping of the modulator [6]. As various frequencies are used in different countries the resonator capacitance and thus the center frequency can be tuned digitally. The Q-factor depends on the center frequency so the transconductances $G_m$ and $G_q$ were made configurable as well. All control signals can be written to the control register by a two-wire serial interface and each control word has a length of 5 bits. The control words are transformed by parallel digital-to-analog converters into bias currents of the transconductance stages. The same principle is applied to the switchable capacitance block. The simulated output signal of the modulator for a single-tone sinusoidal input signal at a frequency of 2.14 GHz is shown in fig. 3. The simulated signal-to-noise ratio within a bandwidth of 20 MHz is as high as 59 dB and still 52 dB for a bandwidth of 60 MHz. The circuit is implemented in a SiGe bipolar technology from Infineon with a transit frequency beyond 200 GHz. The chip area is 2.2 mm² and consumes about 1 W at a supply voltage of 3.1 V.

III. DRIVER AMPLIFIER

The required output power of mobile base stations can be larger than 100 W at about 2 GHz operating frequency. Therefore, the transistors of a switching amplifier should exhibit transit frequencies beyond 100 GHz and breakdown voltages well above 10 V. For the time being only III/V-transistors are promising candidates for this application. As those transistors are typically depletion type, a large voltage swing is required to drive these transistors. Hence, a driving amplifier is also designed in a SiGe bipolar technology, however transistors with larger breakdown voltage are required and complementary transistors simplify the circuit design. Therefore the special process option from the IHP is chosen offering an npn transistor with an $f_t/f_{max}$ of 110 GHz/180 GHz and a pnp transistor with an $f_t/f_{max}$ of 90 GHz/120 GHz.

The block diagram of the H-bridge driver amplifier is shown in fig. 4. The differential input signal from the modulator is preamplified and levelshifted by a current-mode logic input stage. Then two-stage inverters are increasing the voltage swing to drive the push-pull output stages. Both halves of the bridge are identical in design, however, they are steered by inverse signals. In H-bridge configuration the differential output signal between the two output nodes of the push-pull stages is fed into the bandpass filter to reconstruct the amplified RF signal. Alternatively, the output signal can be used as a differential input signal for a GaN power amplifier.

The challenge in the design of switching amplifiers is to reduce the switching losses by direct path currents during switching and the dynamic consumption by charging and discharging of the output node capacitance. Thus, short rise and fall times are required which is challenging the transistor technologies. However, transit frequency and breakdown voltage in a device are contradictory in their scaling requirements. The chosen complementary bipolar technology is a good compromise for moderate output power at GHz operating frequencies. The simulated pulse train for a 1.6 GHz input signal is shown in fig. 5.

Figure 3. Simulated output spectrum for a sinusoidal input signal at 2.14 GHz. The dashed lines mark the center frequency $f_c$ and frequencies with ±10 MHz offset from $f_c$.

Figure 4. H-bridge driver amplifier.

Figure 5. Simulated pulse train of a bandpass delta-sigma modulated signal at a clock frequency of 6 GHz.
The output voltage swing of 3 V is sufficient to drive a GaN power amplifier. The rise and fall times of the output signal are about 30 ps. The DC power consumption of the driver amplifier is 283 mW for the simulated delta-sigma modulated signal and the output power is 120 mW. As the input power is only 1.5 mW a power added efficiency of 41.9 % is calculated for the driver amplifier. The output power of a mobile terminal can be achieved by applying several output stages of the H-bridge in parallel. The simulation results demonstrate the feasibility of the class S concept. Further improvements of the output power and the efficiency can be obtained by advanced transistor technologies and optimized circuit design.

IV. EXPERIMENTAL RESULTS

The modulator chip is already fabricated and tested using a Rohde & Schwarz SMF-100A for clock generation and a SMU-200 for sinusoidal and modulated RF input signals and the spectrum analyzer FSQ-8. 180°-hybrid directional couplers are used for single-ended-to-differential conversion for the clock and the input signal and for the differential-to-single-ended conversion of the output signal [7]. The clock frequency for all measurements is 7.5 GHz.

In fig. 6 the measured modulator output spectrum is shown for a two-tone input signal at 2.2 GHz with 6 MHz offset. Clearly the noise shaping function of the bandpass delta-sigma modulator can be seen. The measured single-ended output voltage swing is 250 mV. The output signal and noise power in a bandwidth of 20 MHz for a single-tone input signal at 2.2 GHz are plotted in fig. 7 versus the input power. There is a large range of linear operation from - 40 dBm input power up to about - 8 dBm where an abrupt change to the saturated output power occurs demonstrating the high linearity of the BPDSM. The noise power density is measured at 10 MHz offset from the carrier. The noise power is flat in a bandwidth of more than 25 MHz around the carrier. The measured peak SNR is 45.5 dB in a bandwidth of 20 MHz.

The tunability of the BPDSM is shown in fig. 8. The output power as well as the corresponding noise power in a bandwidth of 20 MHz are measured at peak SNR across a center frequency of the modulated input signal from 1.55 GHz up to 2.45 GHz. Output power as well as noise power keep almost constant for the whole tuning range. The measured power consumption increases moderately from 992 mW at 2.45 GHz center frequency up to 1.27 W at 1.55 GHz. The increase in power consumption at lower frequencies is caused by the switched-on resonator capacitances.
V. CONCLUSION

A CT BPDSM is designed and fabricated for operation frequencies from 1.55 GHz up to 2.45 GHz. A driver amplifier using also SiGe bipolar transistors is designed as an intermediate stage to a high power GaN output stage. The high linearity of the BPDSM with a power consumption of about 1 W offers the chance to build class-S amplifiers for mobile base station applications with high efficiency.

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