A Pipelined 3-Level Bandpass Delta-Sigma Modulator for Class-S Power Amplifiers

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Abstract—A digital bandpass delta-sigma modulator for class-S power amplifiers is presented. In comparison to a 2-level modulator coding efficiency can be increased by 10% over a large input power range with a 3-level modulator. Scaling the quantizer thresholds offers a trade-off between coding efficiency and signal-to-noise ratio.

The bandpass modulator architecture allows twofold interleaving. A constraint on the quantizer thresholds and the feedback values reduces the effective operand word width in the feedback loop to the 5 most significant bits. Pipelining of the less significant bits leads to a short critical path. Interleaving and pipelining promise fast operation and thus a high maximum signal frequency.

I. INTRODUCTION

Mobile communications have experienced a rapid development in the last decade which lead to many new standards. One of the key challenges for the suppliers is to develop a flexible RF transmitter architecture which offers access to multiple standards and frequency bands.

Analog transmission chains are presently limited to and optimized for one frequency band. Important components like mixers and filters are inherently frequency dependent. Optimization of the matching network for the power amplifier (PA) is done for a narrow frequency band to ensure lowest noise level and best power efficiency.

A class-S amplifier with bandpass delta-sigma modulator is considered to be an attractive solution for frequency agile transmitters (Fig. 1). Signal processing from baseband to RF is done in digital domain which saves power and offers maximum flexibility. Further advantages of the digital design are higher yield and less effort for migration to other technologies.

A switching-mode amplifier converts the signal from digital to analog domain. Again the signal frequency is bounded only by the maximum switching frequency of the amplifier. Switching-mode amplifiers are in active development and achieve already switching rates of more than 6 Gb/s [1], [2]. In contrast to single-ended amplifiers H-bridge amplifiers offer an additional “idle” state which can be used in 3-level modulators. The integration of the amplifier and the modulator on a single die is not yet feasible because of the low supply voltage and the resulting low maximum output power of advanced CMOS nodes. Therefore the output word width of the modulator should be as small as possible to reduce complexity of the interface and the output stage and avoid timing problems known from multi-bit digital-to-analog converter architectures.

The last component of the class-S amplifier is the reconstruction filter which has to offer a high Q-factor and low losses.

This article presents an architecture for a 3-level modulator for mobile communications in the GHz range. Sommarek [3] presents a 4th-order bandpass delta-sigma modulator with a special pipelining architecture which reaches a clock frequency of 700 MHz. A 3rd-order lowpass delta-sigma architecture with subsequent IQ-modulation achieves a clock frequency of 4 GHz with a signed-digit number representation [4]. Both architectures operate with a sampling rate which is 4 times the signal frequency leading to a maximum signal frequency of 175 MHz and 1 GHz. Transmission on the first image band triples the possible signal frequency but reduces the coding efficiency significantly. As a result a more powerful PA is required and the power efficiency drops. Thus, current CMOS implementations of the modulator are still too slow for mobile communication standards with carrier frequencies around 2 GHz. As an intermediate approach analog modulators in bipolar technology are fast enough but frequency dependent and exhibit high power consumption [5], [6].

This article concentrates on modulator architectures for mobile communications in the GHz range. Mobile communications in the GHz range. This article presents an architecture for a 3-level modulator with better coding efficiency and competitive maximum signal frequency. The paper is organized as follows: A comparison between 2-level and 3-level operation of a 4th-order modulator is given in Section II. Special attention is paid to signal-to-noise ratio (SNR) and coding efficiency. Section III discusses the implementation of the modulator using interleaving and pipelining techniques. Section IV concludes the article.

II. MODULATOR DESIGN

Fig. 2 shows the block diagram of a 4th-order 16-bit BPDSM. The model employs the cascade of resonators topol-
ogy with two $z^{-2}$ resonators. The architecture with a value of $k = 1$ is called the standard 3-level architecture in the following. The feedback value is provided by a multiplexer which is controlled by the quantized output signal. In case of a 2-level modulator the feedback values are $\pm 4096$, in case of a 3-level modulator the feedback values are $\{+4096, 0, -4096\}$.

For a 2-level modulator the quantizer is a simple comparator with threshold zero. For a 3-level modulator a quantizer with two thresholds at $\pm 4096$ is used.

As indicated in the introduction coding efficiency is an important measure for class-S amplifiers. Coding efficiency $\eta_k$ is defined as the ratio between signal power $P_{\text{sig}}$ and total output power $P_{\text{tot}}$

$$\eta_k = \frac{P_{\text{sig}}}{P_{\text{tot}}} \quad (1)$$

In case of a 2-level modulator the output pulsetrain consists of the output values $\{-1, +1\}$. Thus the total output power $P_{\text{tot}}$ is constant while the signal output power $P_{\text{sig}}$ and the coding efficiency grow with the square of the input amplitude (Fig. 3).

For the standard 3-level modulator both - the signal output power and the total output power - increase with the square of the input amplitude. Therefore, the coding efficiency is proportional to the input amplitude. The peak coding efficiency of the 3-level modulator is as high as 35%. Over a wide input amplitude range it is more than 10% higher than the coding efficiency of the 2-level modulator.

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The spurs can be seen as a drop in the signal-to-noise ratio (SNR) vs. bandwidth relationship in Fig. 5. The SNR for $k = 4$ approaches the SNR of the 2-level modulator. The SNR for $k = 2$ shows less spurs and even achieves a higher SNR than the standard 3-level modulator for large bandwidths. The spur which results in a drop in the SNR vs. bandwidth for the 2-level modulator is even higher in the 3-level modulator with $k = 1/2$.

The behavior for large input signals can be explained as follows: Larger values of $k$ lead to more nonzero decisions of the quantizer. For very large values of $k$ the quantizer does no longer detect zeros and becomes equivalent to the 2-level modulator. For medium values of $k \approx 1\ldots2$ the number of decisions is approximately equal for all three output levels and the SNR is best. The smaller the values of $k < 1$ the more zero decisions will occur. More spurs will be visible on the spectrum and nonlinearities appear.

In conclusion $k = 1$ is an attractive compromise between SNR and coding efficiency and is chosen for the modulator architecture. For systems with larger bandwidth $k = 2$ offers less spurs and thus a slightly larger SNR at the expense of a reduced coding efficiency.

III. MODULATOR ARCHITECTURE

Pipelining and interleaving are frequent solutions to increase the throughput of digital signal processors [7]. Pipelining is a technique where arithmetic operations are divided into smaller operations which are separated by registers. That leads to an increased latency in terms of clock cycles per operation but...
allows for a higher overall clock rate. Usually, feedback systems cannot be pipelined because the introduction of additional registers changes the transfer function of the system.

For memoryless systems interleaving can be used to parallelize the computation. The process flow is blockwise: A demultiplexer divides the data stream into several independent data streams. All streams are processed at the same time. At the end the output signal is reconstructed by combination of the data streams in the right order.

A. Time-Interleaving Architecture

The proposed bandpass delta-sigma modulator is a feedback system with memory and a nonlinear quantizer. The quantizer prevents reordering of the operations and thus arbitrary parallelization. However, the two $z^{-2}$ resonators are implemented with two registers in series. Odd (even) output symbols only depend on odd (even) input symbols. Therefore, the modulator can be split into two parts processing odd and even symbols separately (Fig. 6). This doubles the maximum output data rate.

B. Pipelining of Modulator Core

While block A in Fig. 6 can be pipelined on bit or subword level, general pipelining is not applicable to the modulator architecture as a whole due to feedback. However, if the quantizer thresholds are large powers of two, the less significant bits are outside the feedback loop and can be pipelined.

The coefficient $k$ is implemented by scaling the quantizer thresholds with $1/k$. The larger the quantizer thresholds the smaller the wordwidth the quantizer has to take into account and thus the faster the implementation. For $k = 1$ the quantizer thresholds are:

\[
\begin{align*}
0 & \quad \text{or in two’s complement} \\
+4096 & \quad 00010 00000 000000 \\
-4096 & \quad 11110 00000 000000
\end{align*}
\]

The five most significant bits (MSB) are sufficient for proper quantization with 3-levels and $k = 1$. The remaining eleven less significant bits can be pipelined (Fig. 8). The maximum word length of the pipelined ripple carry adders is determined by the critical path of the feedback loop. The extra delay due to the quantizer and the multiplexer is large, thus the adder for the eleven bits can be split into a 5-bit adder and a slower 6-bit adder.

For maximum speed the quantizer, the feedback multiplexer and the 3-input adder have to be optimized. The two quantizer output bits represent sign and magnitude. The sign value is equal to the MSB of the input word. The magnitude bit can be implemented with the combinatoric net in Fig. 7.

The feedback value is generated with a two-stage multiplexer controlled by the two quantizer bits. The first stage is directly controlled by the sign bit and thus outside the critical path.

The 3-input adder in the feedback path receives inputs from the preceding stage, from the local feedback loop and from the global feedback loop (Fig. 9). The local inputs are fed into the first adder column because they are immediately available at the rising clock edge. The global feedback exhibits a larger delay than a single sum delay and is added in the second adder column. The word width of the second adder can be reduced to four bits for the subtraction and three bits for the addition because only the four MSBs of the feedback value are nonzero.

C. Timing of Critical Path

The critical path includes the quantizer, the feedback multiplexer and the 3-input ripple carry subtractor. The critical delay
of the quantizer is equivalent to the delay of two XOR gates and one multiplexer. Two CMOS inverters are used to properly drive the feedback multiplexer. The subtractor accounts for an inverter delay for inversion of the two’s complement, three carry delays and one sum delay.

\[
\begin{align*}
t_{\text{critical path}} &= t_{\text{quant}} + t_{\text{fbMUX}} + t_{\text{3input-subtractor}} \\
\text{with } t_{\text{quant}} &= 2t_{\text{XOR}} + t_{\text{MUX}}, \\
t_{\text{fbMUX}} &= 2t_{\text{INV}} + t_{\text{MUX}}, \\
t_{\text{3input-subtractor}} &= t_{\text{INV}} + 3t_{\text{carryRCA}} + t_{\text{sumRCA}}.
\end{align*}
\]

IV. CONCLUSION

A fast 3-level bandpass delta-sigma modulator is presented. 3-level operation of the modulator is analyzed with respect to coding efficiency and SNR. Different 3-level modulators are compared to each other and to a 2-level modulator. The 3-level modulator shows a higher SNR for large bandwidths and a 10% better coding efficiency over a large input power range.

An architecture for high throughput is discussed. On the one hand it relies on twofold interleaving of the modulator core. On the other hand it relies on pipelining. A constraint on the feedback to three distinct values allows to reduce the effective word width in the feedback loop to the five most significant bits. The less significant bits are pipelined with 5-bit and 6-bit ripple carry adders. The resulting architecture minimizes the critical path yet retains a low overall complexity and power consumption. An implementation in 65 nm CMOS which is fast enough for signal frequencies above 2 GHz seems feasible.

REFERENCES