Sampling Receive Equalizer with Bit-Rate Flexible Operation up to 10 Gbit/s

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Motivation (1): Applications

Computer mass market, i.e. processor –memory interface
DDR3 ~1 Gbit/s FBDIMM 4.8 Gbit/s
tomorrow: 7 to 10 Gbit/s
transmission length: 2 to 20 cm

Optical networks, i.e. LAN, MAN and WAN
today: 2,5 to 10 Gbit/s
tomorrow: 40 to 100 Gbit/s
transmission length: 10 m to 1000 km

Backplanes, multi-chip modules, i.e. network cross connects, mainframes
today: few Gbit/s
tomorrow: > 10 Gbit/s
transmission length: up to 1m
Frequency Response of 50 Ω Trace on FR4

- 18 dB @ 5.0 GHz
- 19 dB @ 3.0 GHz
- 24 dB @ 3.5 GHz
Measured Single Symbol Time Domain Response

90 cm long trace at 10 Gbit/s

173 cm long trace at 6 Gbit/s
Equalizer Concept (1): Filter Structure

Finite-Impulse-Response (FIR) Filter  removes precursor ISI

Decision Feedback Equalizer (DFE) removes postcursor ISI

analog delays and adding  decision & digital delays

analog weighting
Equalizer Concept (2): Half-Rate Structure

- **Full rate data input**
- **Half rate clock**
- **Half rate demultiplexed**
- **Data outputs**

**FIR-Filter**

**DFE**

- **T&H 1**
- **T&H 2**
- **T&H 3**

**FIR filter adder**

**DFE adder & decision latch**

**D-Latch**

- **Din**
- **CLK**
- **Dout1**
- **Dout2**

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Circuit Design (1): Track & Hold Circuit

bootstrapped clock inputs

CLK/2n  _CLK/2p

V_{in,D}

V_{out,D}

V_{SS}

V_{DD}

I_0

differential complementary transfer gate
optimized for minimum track time

unity gain buffer
optimized for large linear range
Circuit Design (2): FIR Filter Adder

current injection
to ensure constant CM-level

common pair of
load resistors

connected to outputs of interleaved T&H delay chain

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Circuit Design (3): DFE Decision Latch with Adder

DFE analog adder

cross coupled decision latch

from FIR adder

connected to other row decision latch

same row D-latch

(V_{1,D})

(V_{2,D})
Circuit Design (4): Clock Generation

- **CML amplifier**
- **CML divider**
- **CML driver**
- **CMOS driver**
- **Bootstrap circuit**

**INPUT:** $\text{CLK}_\text{in}$

**CML driver for CLK/2 output**

**DIVIDER:** $\div 2$

**CML driver**

**CMOS clock duty cycle control loop**

**OUTPUT:**
- $\text{CLK}/2$
- $\text{CLK}/2p$
- $\text{CLK}/2n$
- $\_\text{CLK}/2p$
- $\_\text{CLK}/2n$
- $\_\text{CLK}/2$
- $\left(\frac{V_{DD} - V_{SS}}{2}\right)$
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Chip Photograph

Input: max. 10 Gbit/s
Output: max. 2x 5 Gbit/s

Chip area: 1400 µm x 600 µm
Core area: 60 µm x 56 µm

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Experimental Results (1): 7 Gbit/s over 173 cm FR4

Loss: 24 dB @ 3.5 GHz
Experimental Results (2): 10 Gbit/s over 90 cm FR4

- 10 Gbit/s
- 10 Gbit/s
- 2x 5 Gbit/s

PRBS $2^{31}-1$

data
clock

diff. trace
FR4 90 cm

equalizer
CMOS 130 nm

Loss: 18 dB @ 5 GHz

coefficient control

oscilloscope, error detector

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Experimental Results: BER versus Sampling Phase

173 cm FR4 trace @ 6 Gbit/s
Loss: 19 dB @ 3 GHz

90 cm FR4 trace @ 10 Gbit/s
Loss: 18 dB @ 5 GHz

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### Performance Summary

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<th>Performance Parameter</th>
<th>Value</th>
<th>Description</th>
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<tr>
<td>Supply voltage $V_{DD}$</td>
<td>1.3 V</td>
<td>$P_{DC}$ equalizer core*</td>
</tr>
<tr>
<td>Maximum bit rate $f_{max}$</td>
<td>10 Gbit/s</td>
<td>$P_{DC}$ clock generator**</td>
</tr>
<tr>
<td>Minimum bit rate $f_{min}$</td>
<td>0.5 Gbit/s</td>
<td>$P_{DC}$ total (with drivers)</td>
</tr>
<tr>
<td>Max. possible channel loss for BER $&lt; 10^{-12}$</td>
<td>24 dB</td>
<td>$P_{DC}$ equalizer core*</td>
</tr>
<tr>
<td>Min. $V_{pp,PPG}$ for BER $&lt; 10^{-11}$, PRBS $2^7$-1, 10 Gbit/s, 90 cm FR4</td>
<td>300 mV</td>
<td></td>
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<tr>
<td>Min. $V_{pp,PPG}$ for BER $&lt; 10^{-11}$, PRBS $2^7$-1, 6 Gbit/s, 173 cm FR4</td>
<td>230 mV</td>
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* Circuitry corresponding to slide 8; ** circuitry in dashed box of slide 13.
Conclusion

• Receive-Side FIR-DFE-Equalizer for up to 10 Gbit/s:
  - small chip area (core: 60 µm x 56 µm)
  - low power consumption (core: 21 mW, clock: 33mW )
  - up to 24 dB channel loss compensation
  - no spiral inductors
  - realized in 130 nm standard CMOS

• Filter frequency characteristic can be shifted continuously by external clock:
  - bit-rate flexible operation
  - especially suited for measurement equipment

• adaptive operation is topic of future work
References


