Mehrpegelmodulation und Entzerrung für Hochgeschwindigkeitsschnittstellen

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unterstützt von

Agilent Technologies Böblingen (Mehrpegelmodulation)
Deutsche Forschungsgemeinschaft (Entzerrer)

Inhalt

- Einführung
  - Eigenschaften eins typischen Backplane-Kanals
  - Vor- und Nachteile der Vierpegelübertragung
  - Entzerrung im Sender- und Empfänger
- PAM4 / PAM2 -Übertragung mit FIR(+DFE)-Entzerrung
  Evaluation auf Systemebene
- PAM2 / PAM4 -Übertragung mit FIR-Entzerrung
  Evaluation auf Schaltplanebene (90nm CMOS)
- PAM2-Übertragung mit FIR+DFE-Entzerrung im Empfänger
  Messergebnisse anhand eines patentierten Entzerrers (130nm CMOS)
- Zusammenfassung

Tyco FR4 Backplane (HM-Zd XAUI Interoperability Platform)

10 GbE XAUI = 2x 4x 3.125 Gbit/s

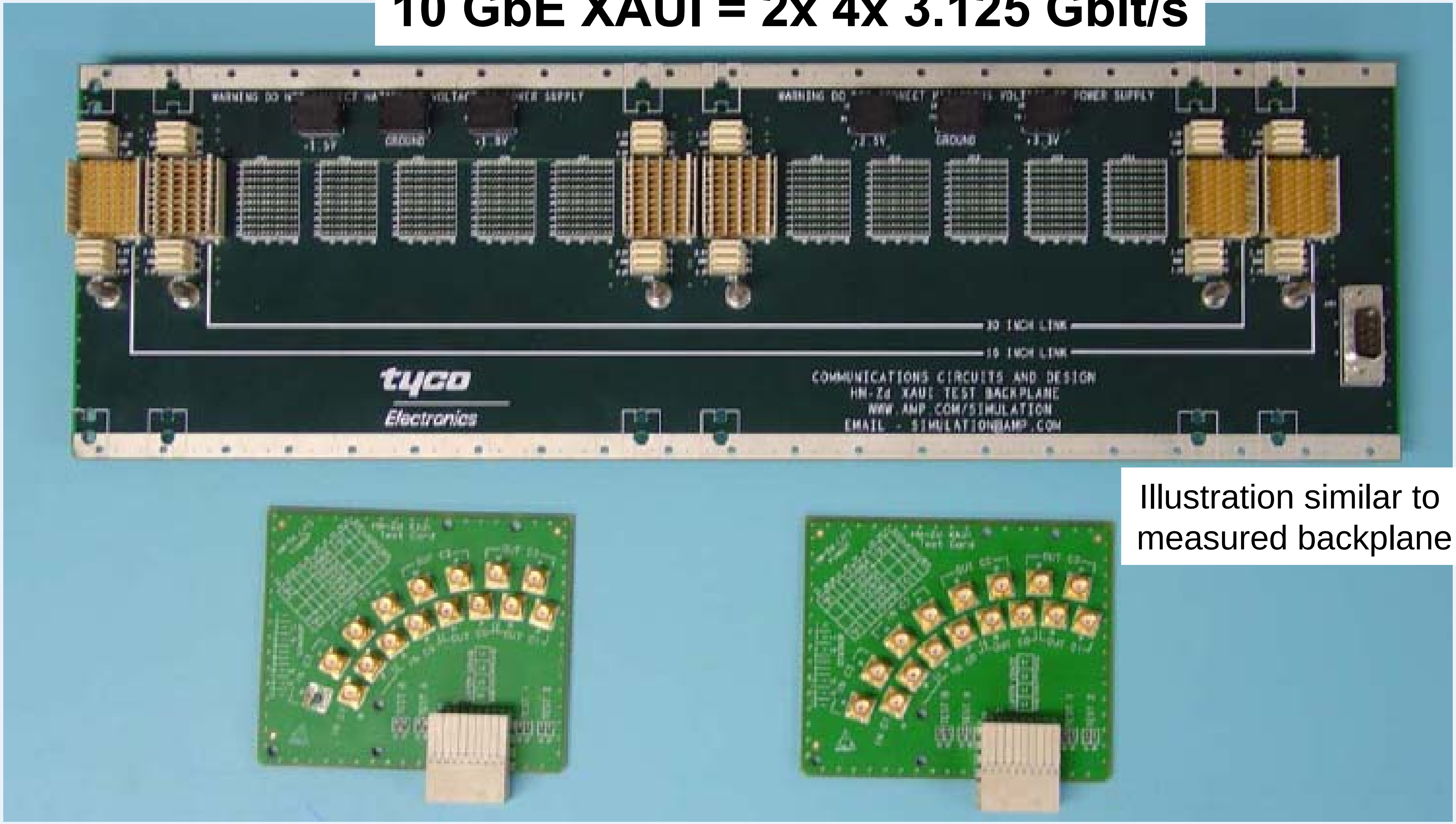
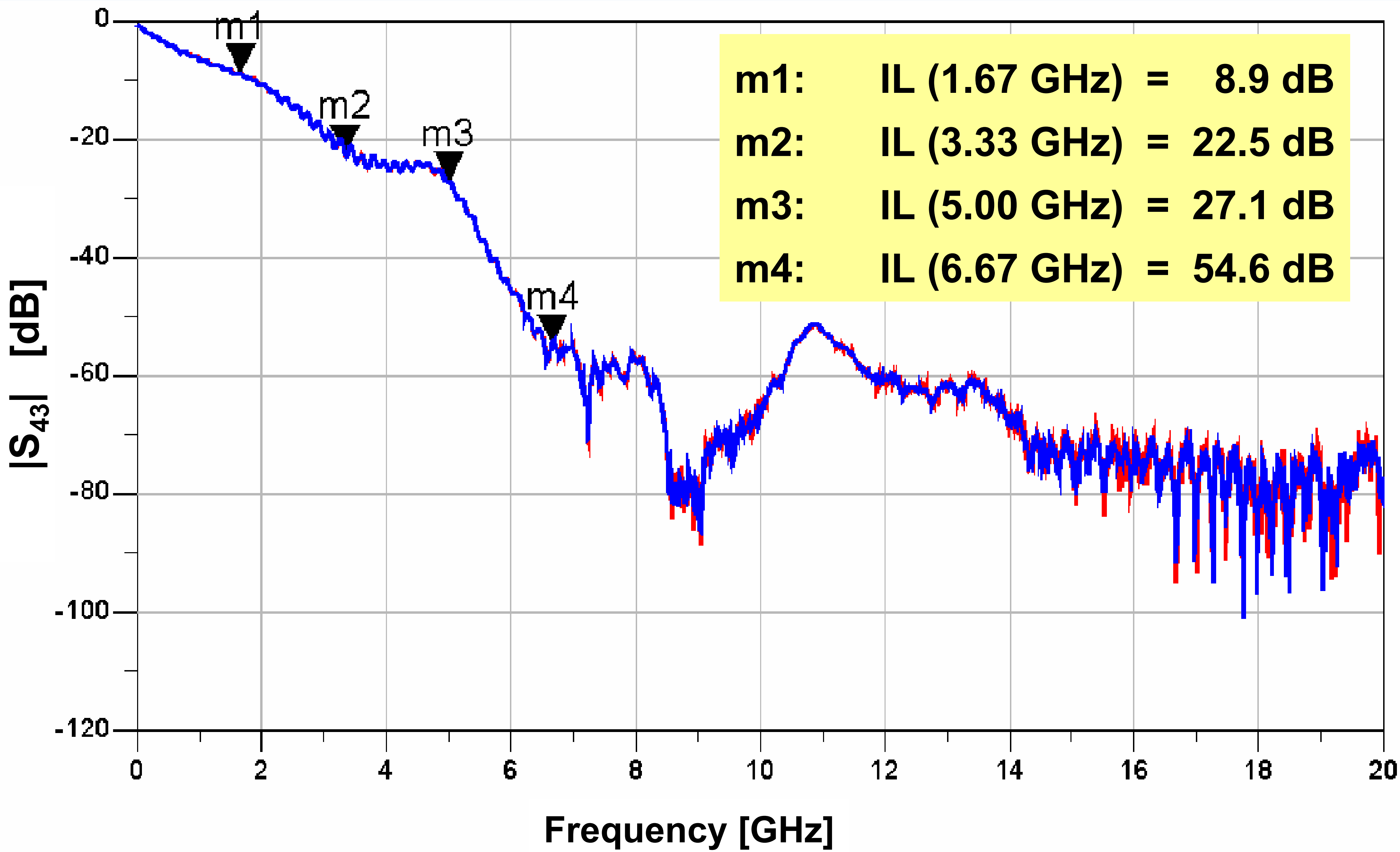


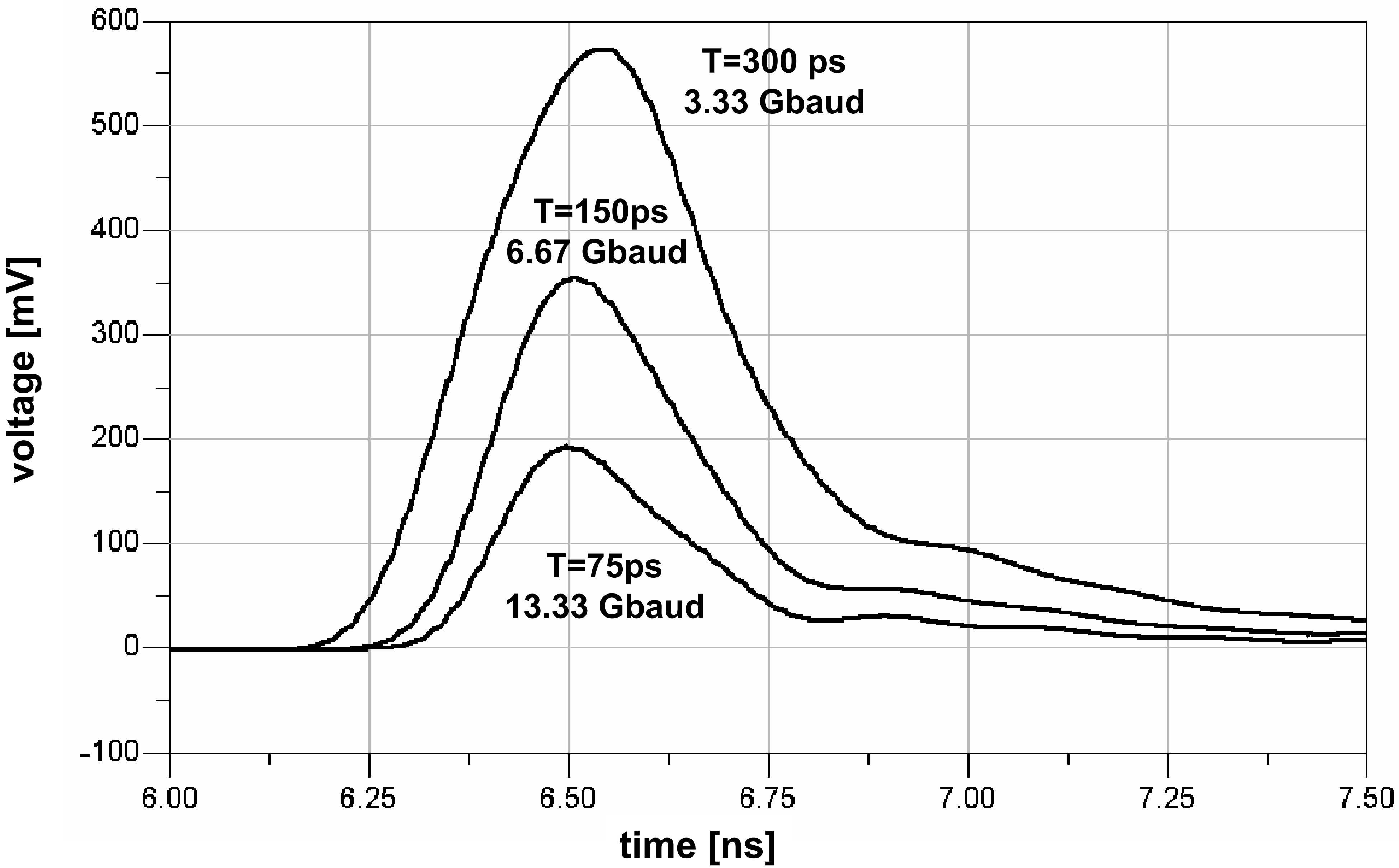
Illustration similar to measured backplane

2x 2in (daughter card) + 30in (backplane) = 34in = 86cm

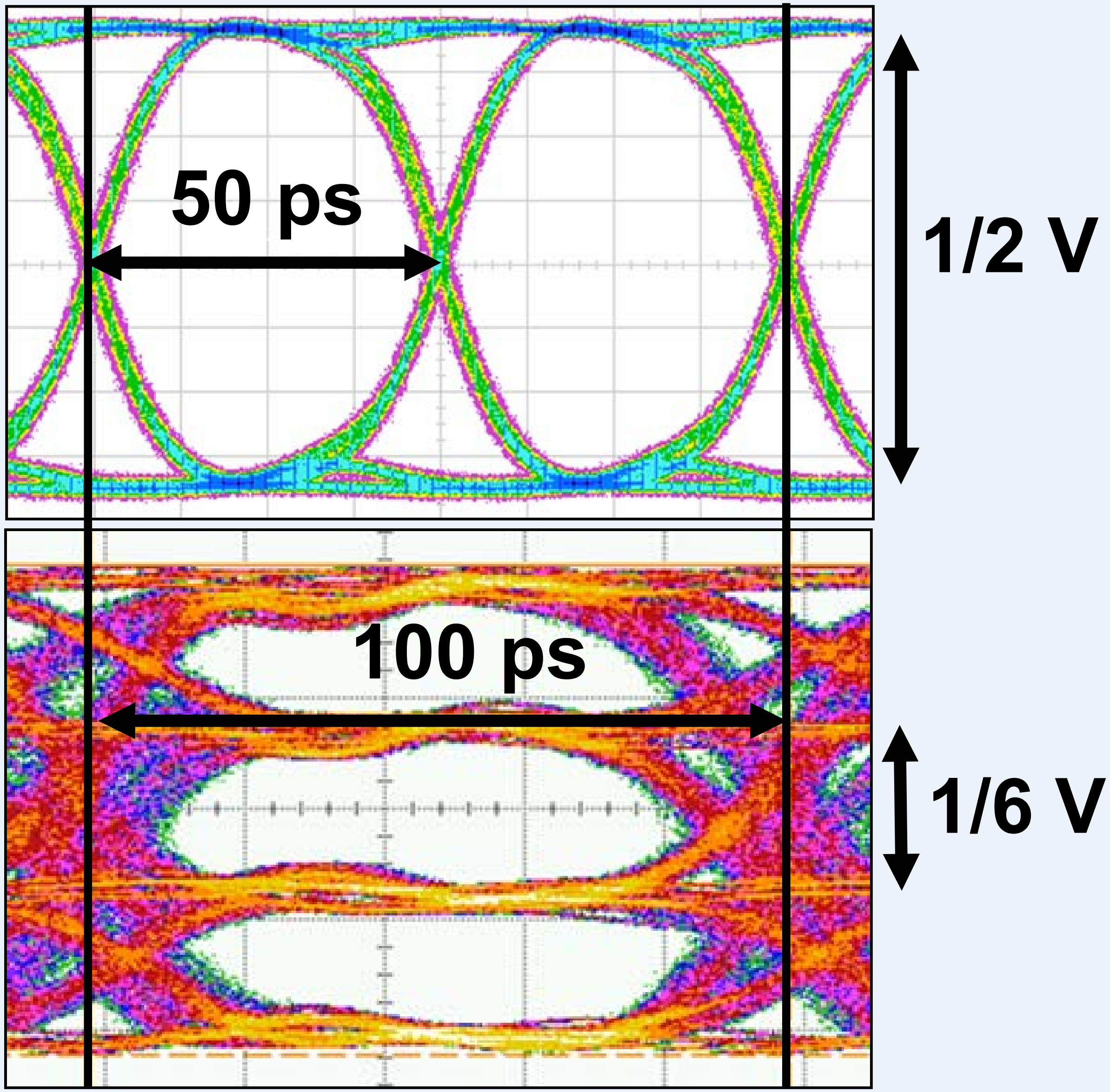
Transmission Characteristic of 86cm Trace



Unit Pulse (1V, 1T) -Response of 86 cm Trace



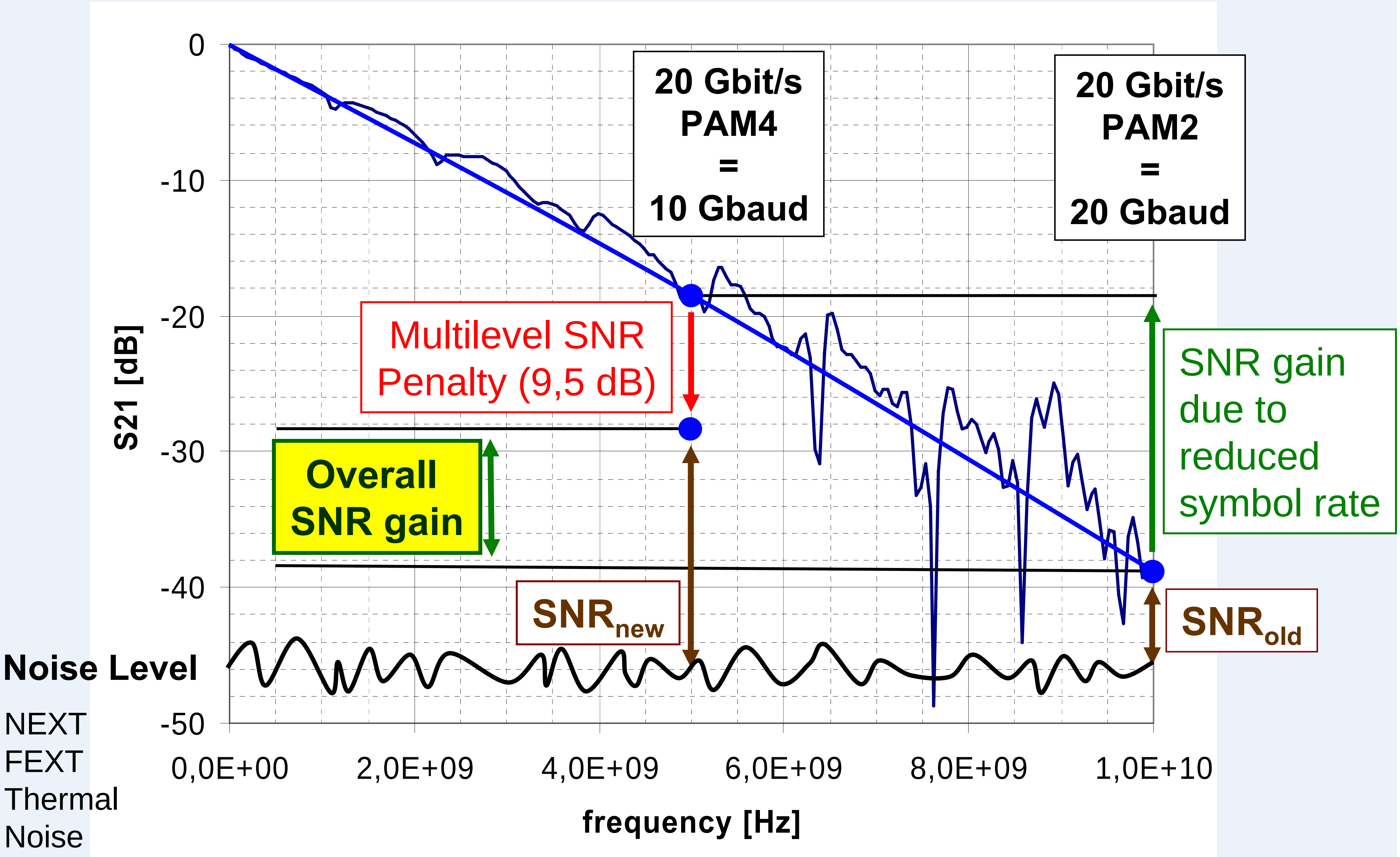
Multilevel Penalty Example: 20 Gbit/s, 0.5 V_{pp}



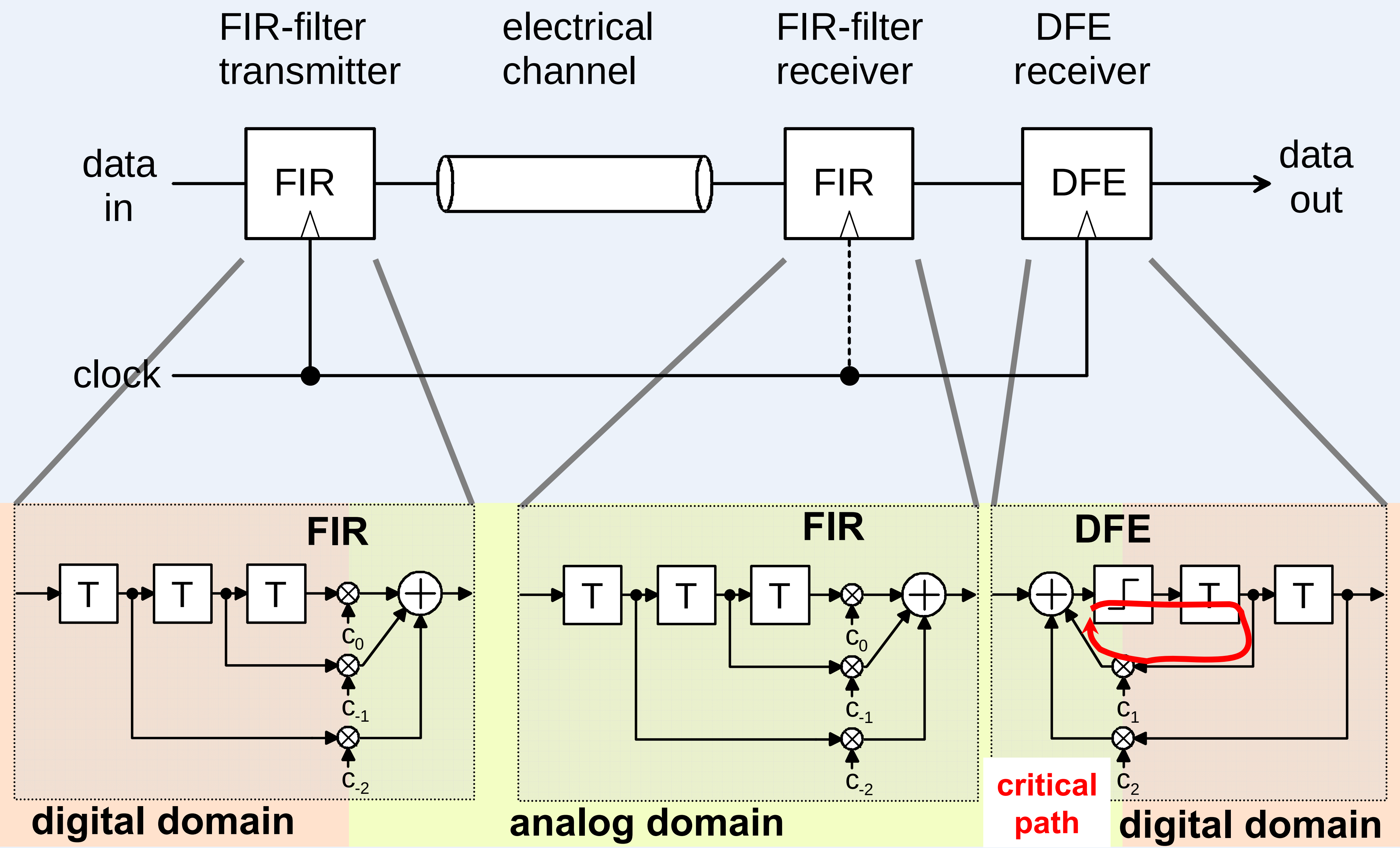
PAM	Signal Power	Eye Area
2	1	1
4	$^1/_9$	$^2/_3$
Penalty	-9.5 dB	-1.8 dB

Picture of PAM4-Eye-Measurement from “Proposals for CEI25 Channels Based on lower-k Dielectric Materials for Backplanes and Daughterboards”, Helmut Preisach, Alcatel Lucent, Stuttgart, OIF-Contribution Number: OIF2007.135.00, Working Group: PLL

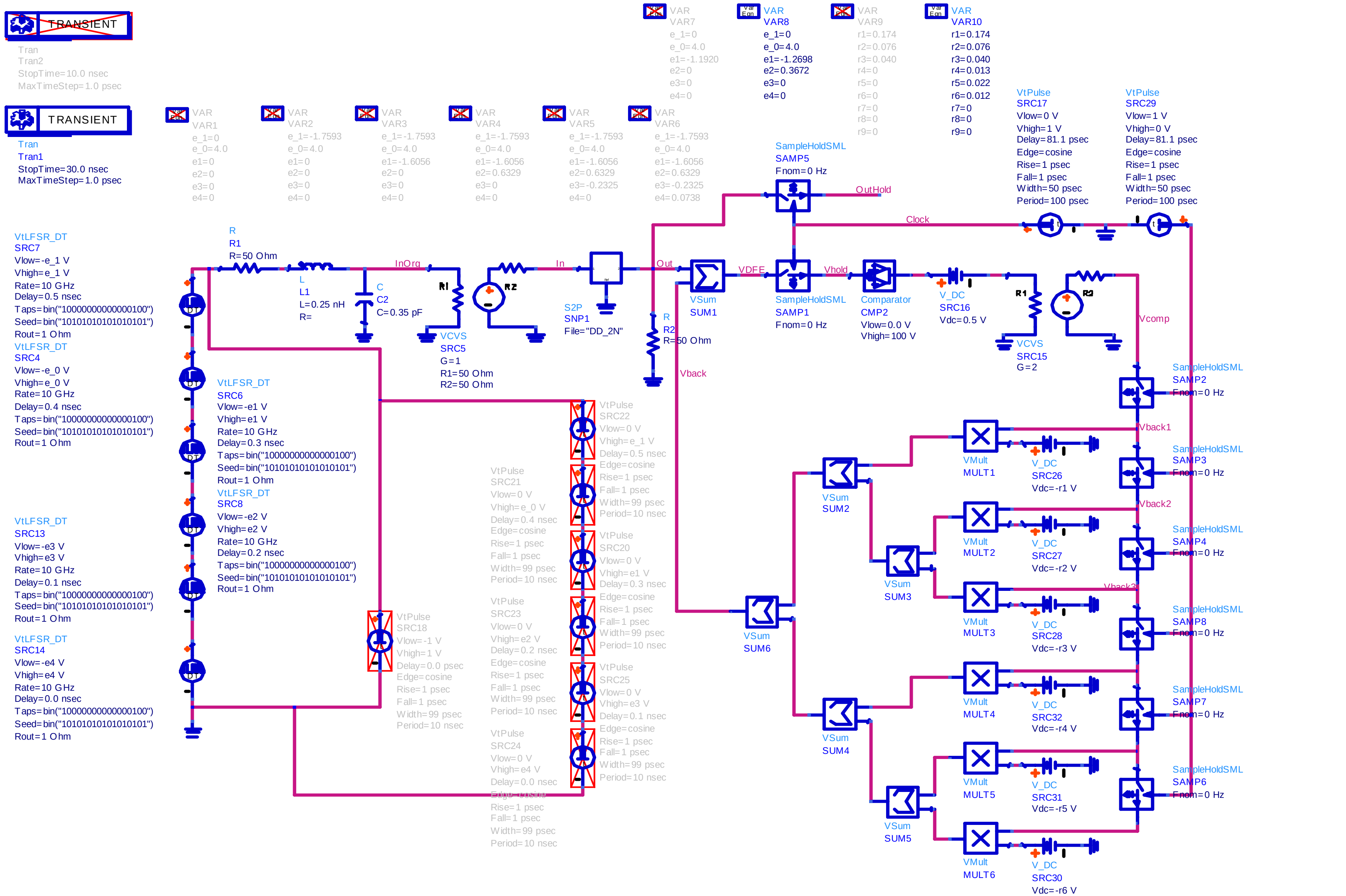
PAM4 Benefit: Consider SNR @ $f_{Nyquist}$



Transmitter & Receiver Equalization



Example of System Simulation Setup in ADS

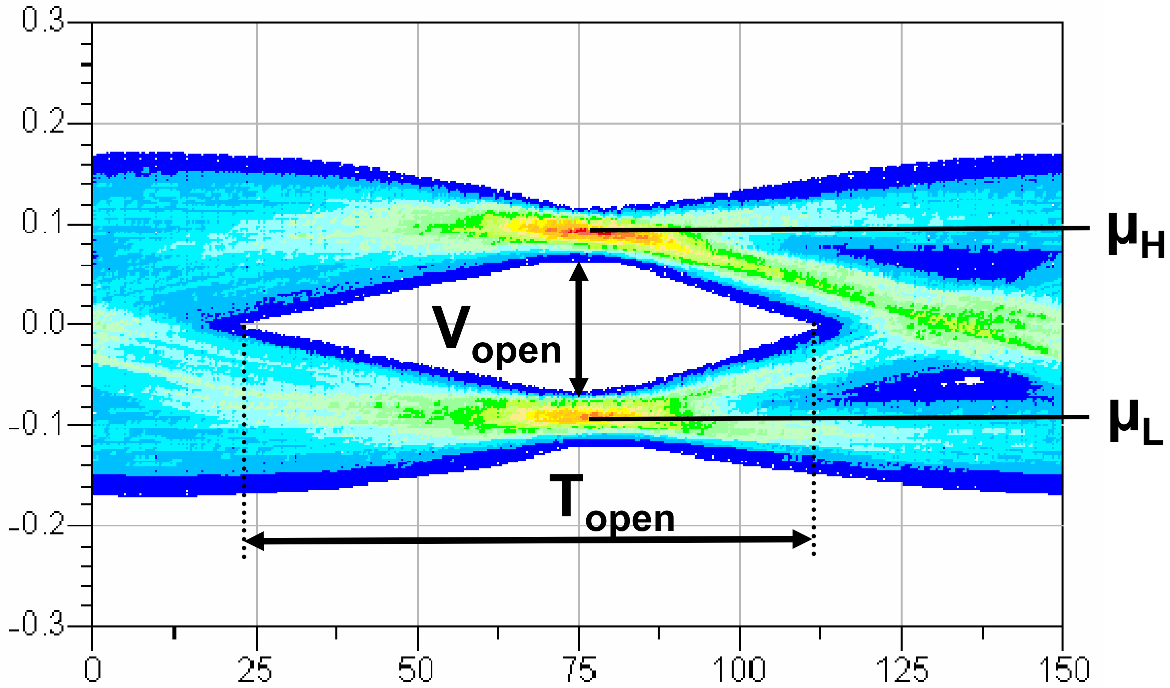


Eye Quality Measures

Eye Area A [in pVs]

$$A \sim \tfrac{1}{2} \cdot T_{open} \cdot V_{open}$$

(~ integrated charge on decision latch input)



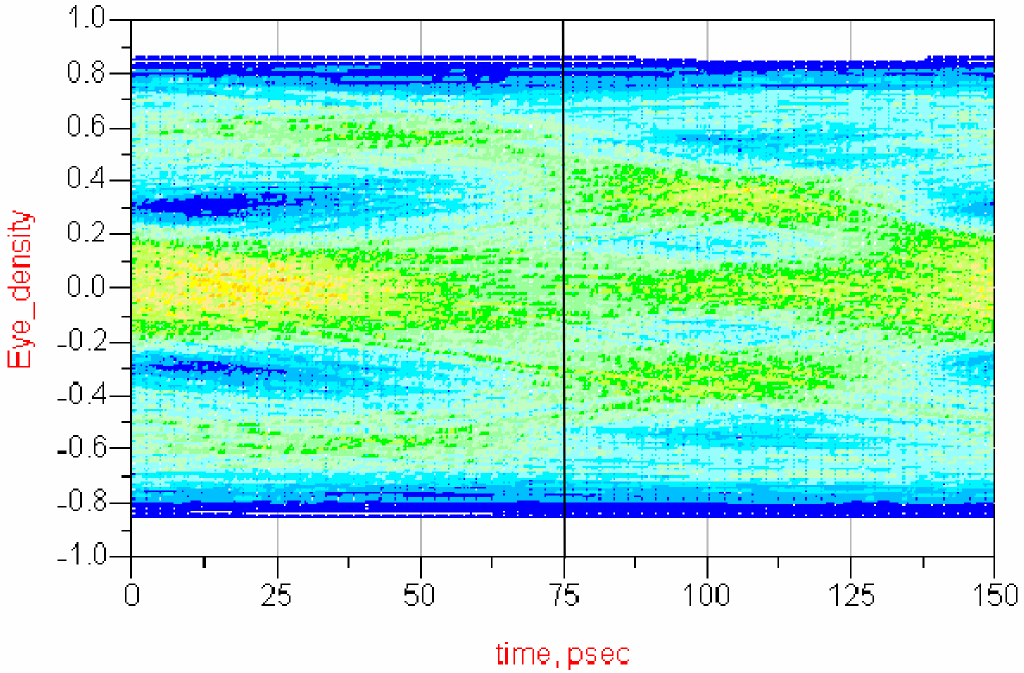
Eye Quality factor Q
(= signal-to-noise ratio at optimum sampling time)

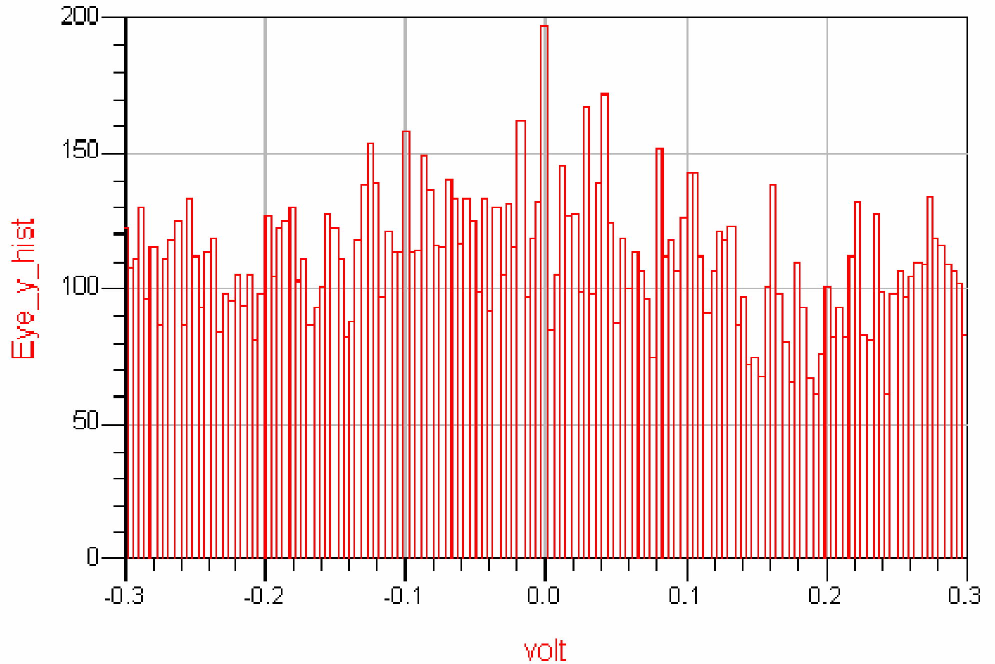
BER estimation from Q-factor
(assuming Gaussian distribution of sampled voltage, is too conservative in most cases)

$$Q = \frac{\mu_H - \mu_L}{\sigma_H + \sigma_L}$$

$$BER = \frac{e^{-\frac{Q^2}{2}}}{Q\sqrt{2\pi}}$$

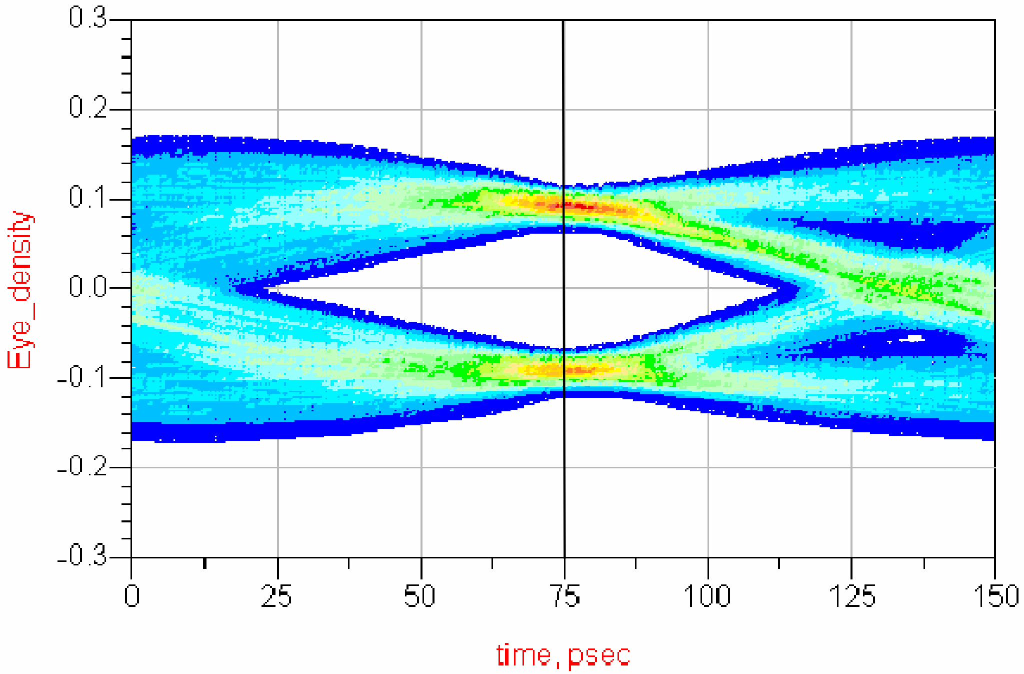
86 cm 6.67 Gbit/s PAM2 FIR (no equalization)

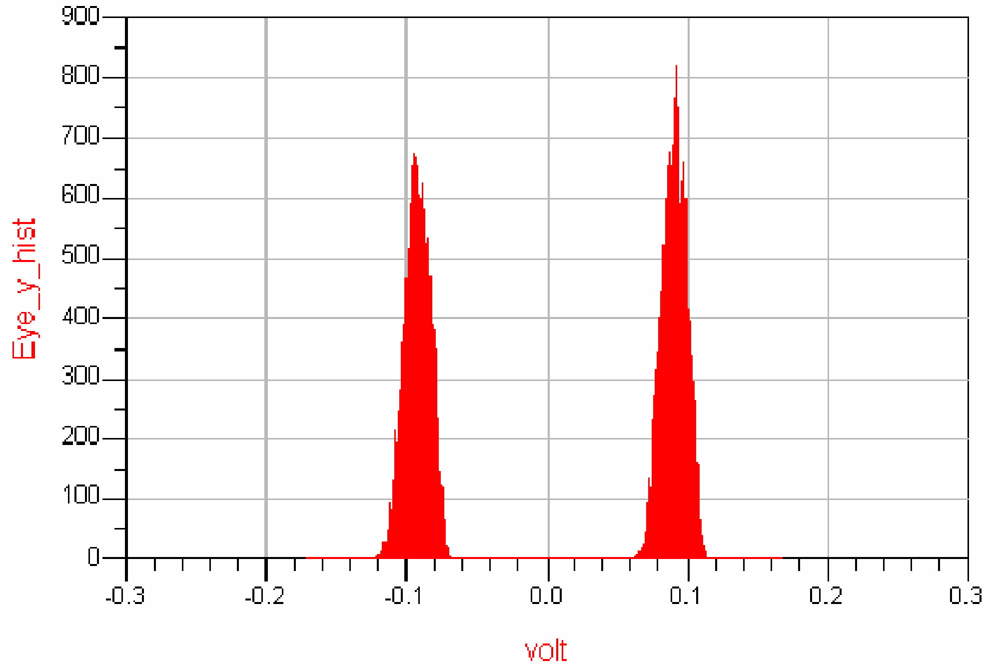




horizontal eye opening	UI	-
vertical eye height	mV	-
eye quality factor Q		-
estimated optimum BER		-

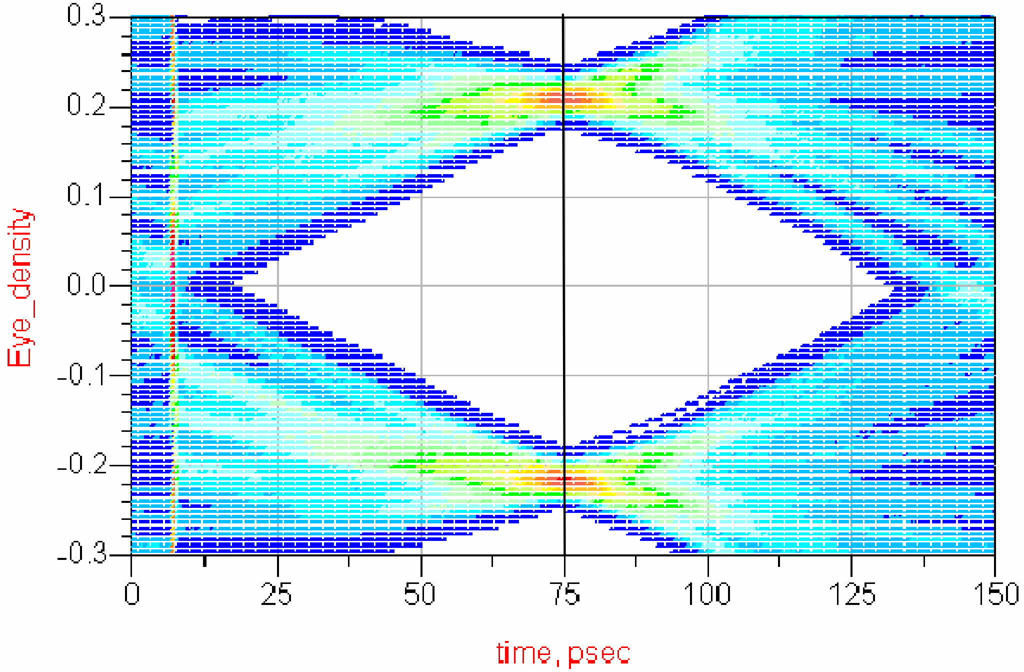
86 cm 6.67 Gbit/s PAM2 FIR (2 Pre-, 3 Post-FIR-Taps)

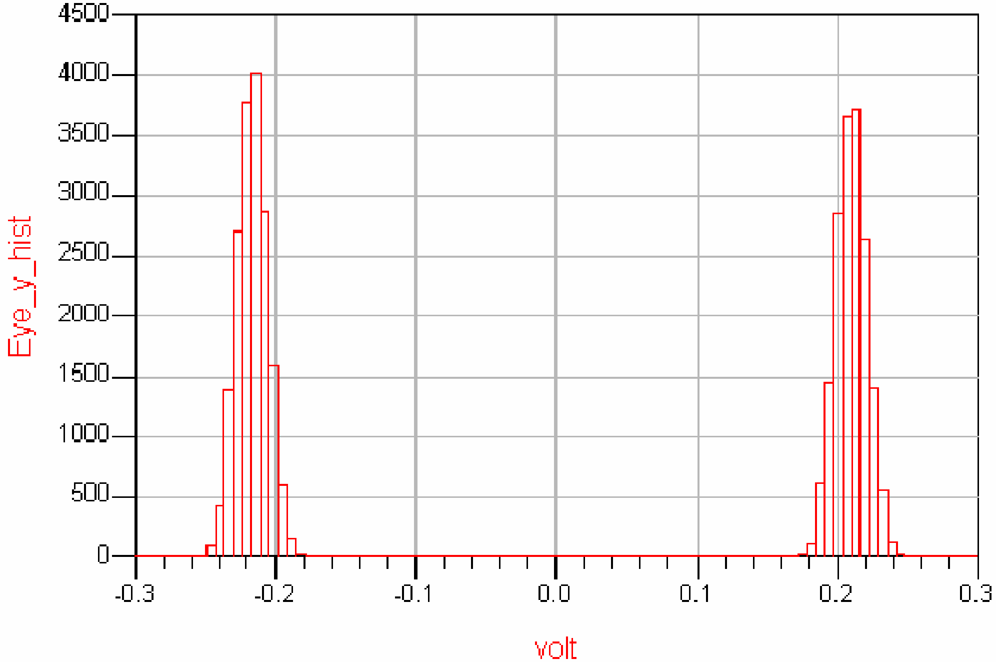




horizontal eye opening	UI	0.58
vertical eye opening	mV	130
eye area	**pVs**	**5.7**
eye quality factor Q		10.3
estimated optimum BER		4.7×10^{-25}

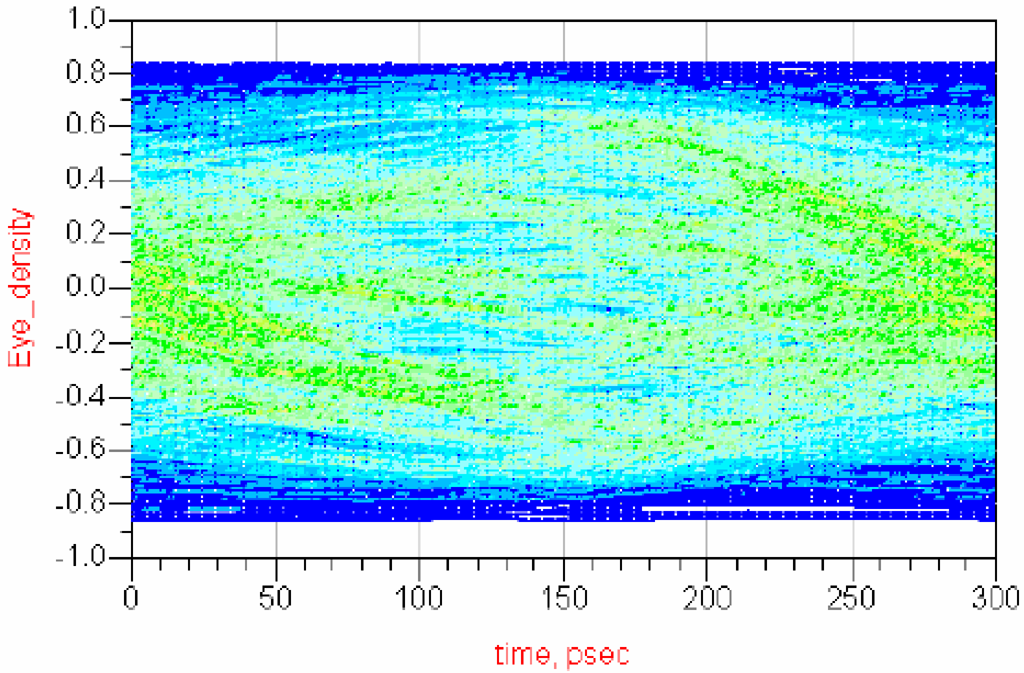
86 cm 6.67 Gbit/s PAM2 FIR+DFE (3 Pre-FIR, 9 DFE-T.)

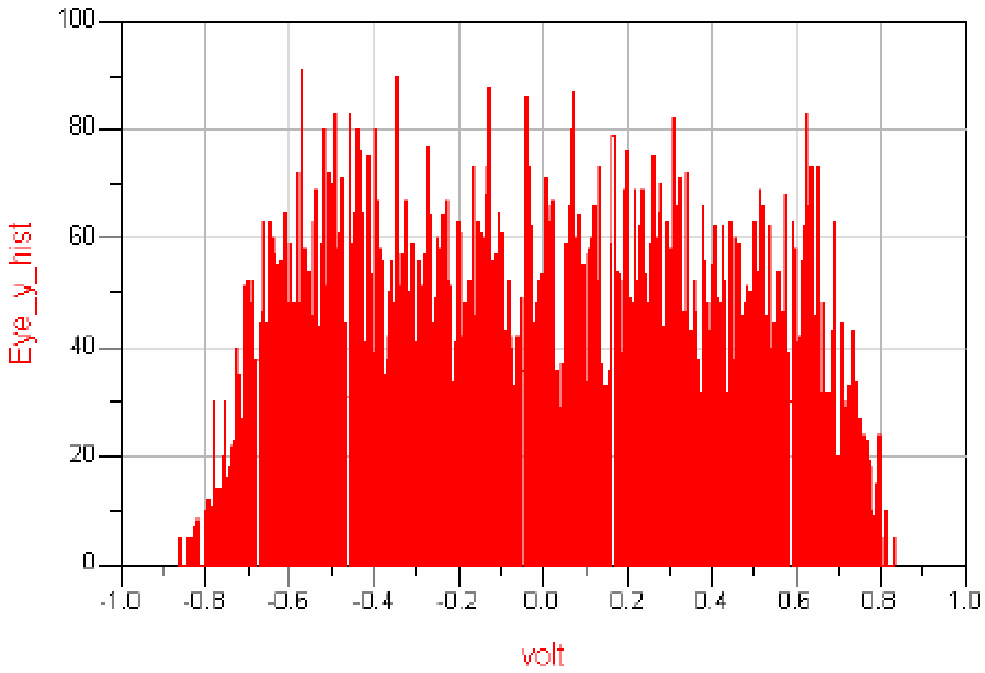




horizontal eye opening	UI	0.75
vertical eye opening	mV	340
eye area	**pVs**	**19.1**
eye quality factor Q		19.4
estimated optimum BER		6×10^{-84}

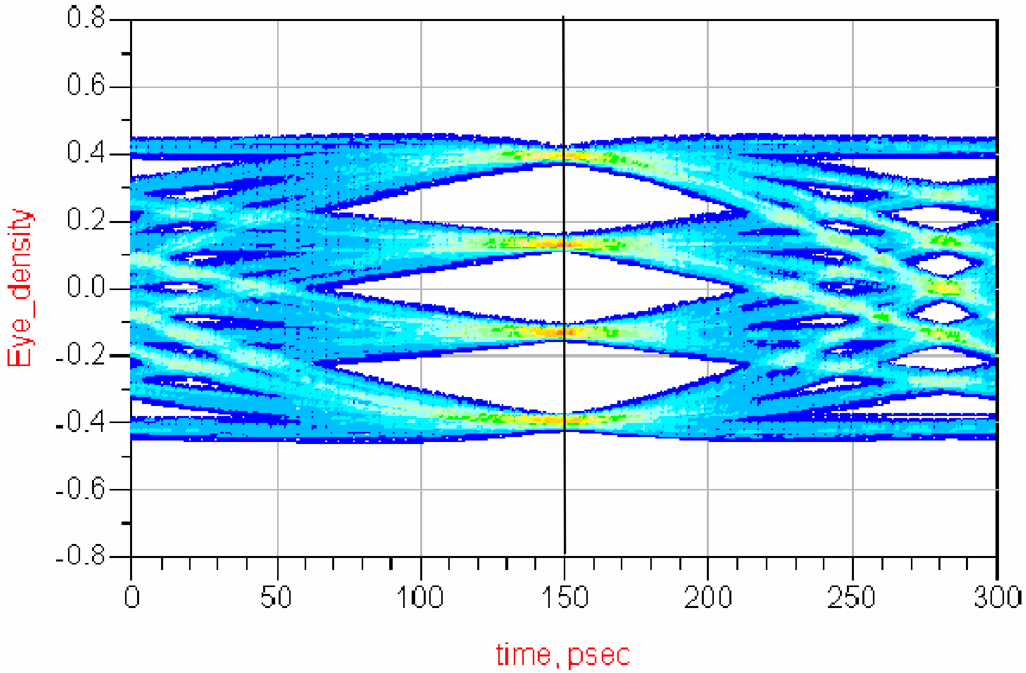
86 cm 6.67 Gbit/s PAM4 FIR (no equalization)

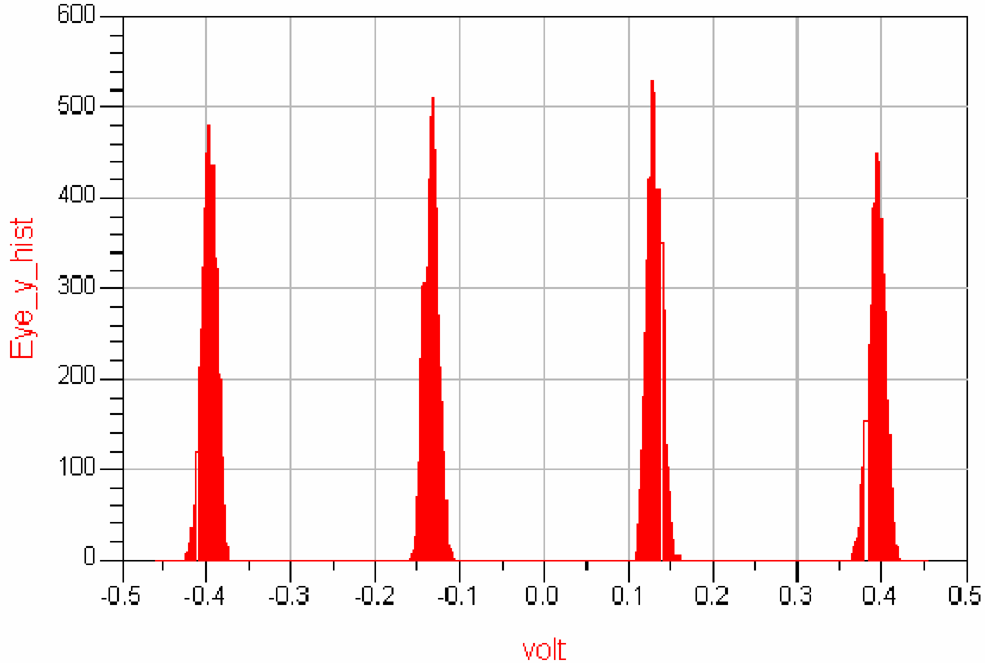




horizontal eye opening	UI	-
vertical eye height	mV	-
eye quality factor Q		-
estimated optimum BER		-

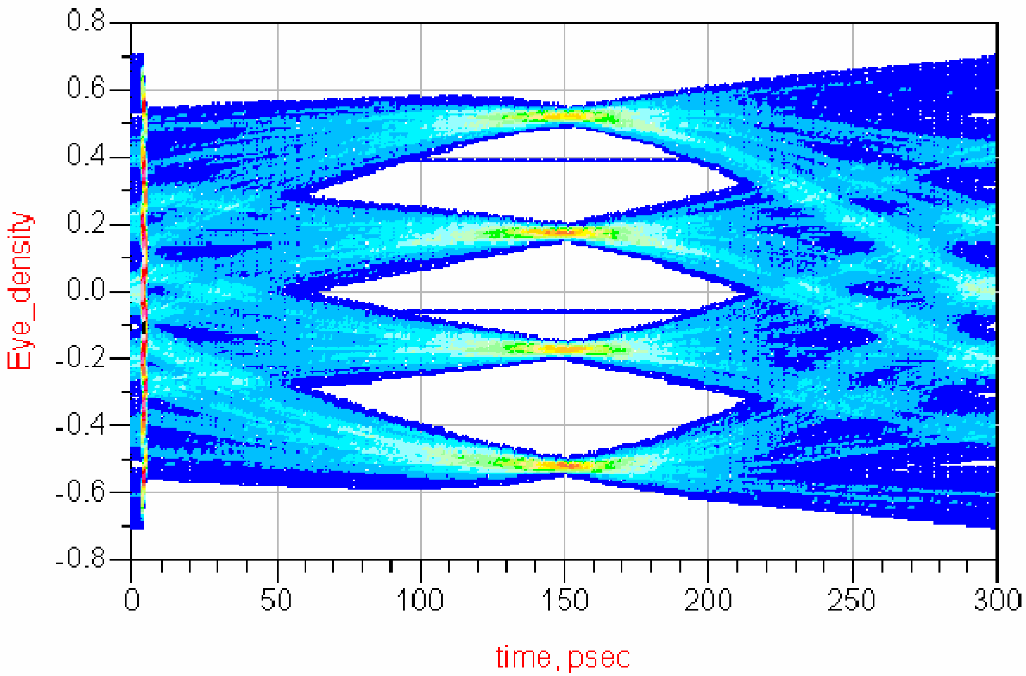
86 cm 6.67 Gbit/s PAM4 FIR (2 Pre-, 3 Post-FIR-Taps)

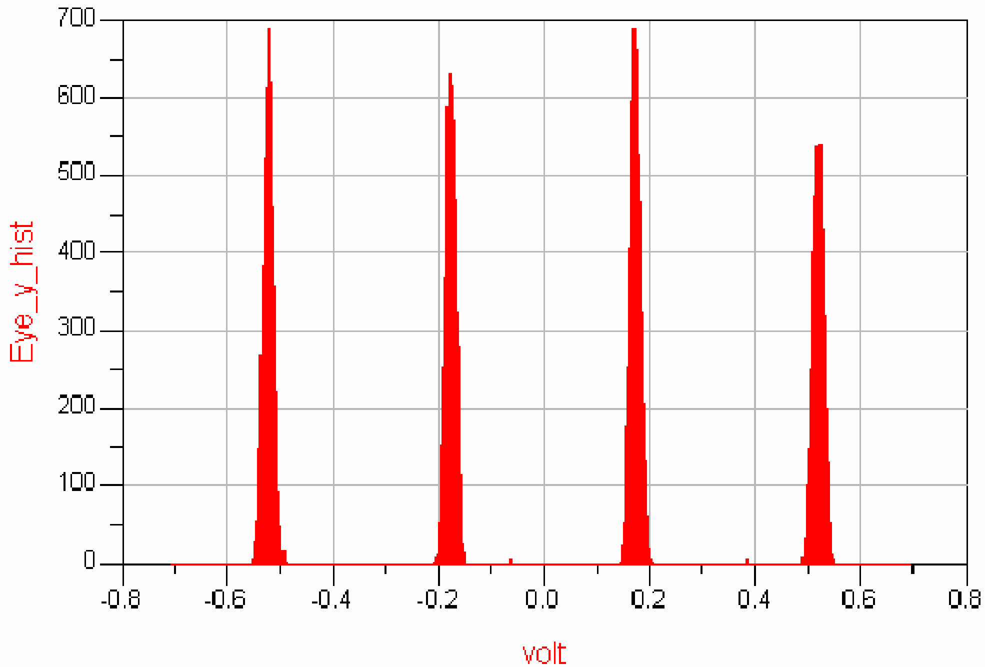




horizontal eye opening	UI	0.46
vertical eye opening	mV	210
eye area	**pVs**	**14.5**
eye quality factor Q		15.1
estimated optimum BER		2×10^{-51}

86 cm 6.67 Gbit/s PAM4 FIR+DFE (3 Pre-FIR-, 9 DFE-T.)





horizontal eye opening	UI	0.45
vertical eye opening	mV	300
eye area	**pVs**	**20.3**
eye quality factor Q		17.0
estimated optimum BER		4×10^{-65}

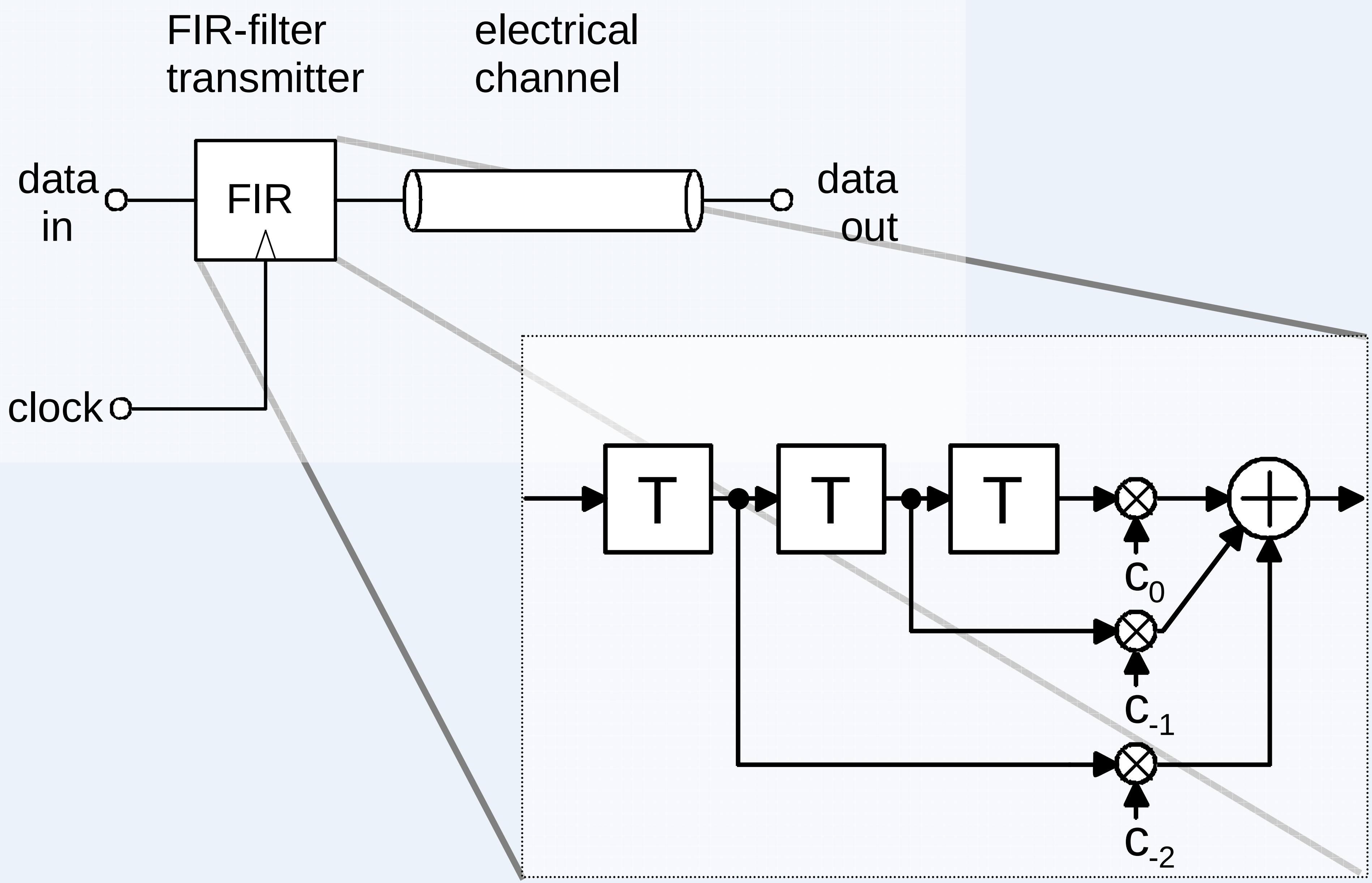
Summary 6.67 Gbit/s Transmission over 86 cm BP

Quality Measure			V_{open}	T_{open}	**A_{open}**	Q
EQ	**Taps**	**PAM**	[mV]	[ps]	[pVs]	
FIR	**1 pre**	**2**	130	72	**4.7**	4.3
	1 post	**4**	170	123	**10.5**	7.1
FIR	**2 pre**	**2**	130	87	**5.7**	10.3
	3 post	**4**	210	138	**14.5**	15.1
FIR	**2**	**2**	290	97.5	**14.1**	9.7
+DFE	**4**	**4**	240	129	**15.5**	11.6
FIR	**3**	**2**	340	112	**19.1**	19.4
+DFE	**9**	**4**	300	135	**20.3**	17.0

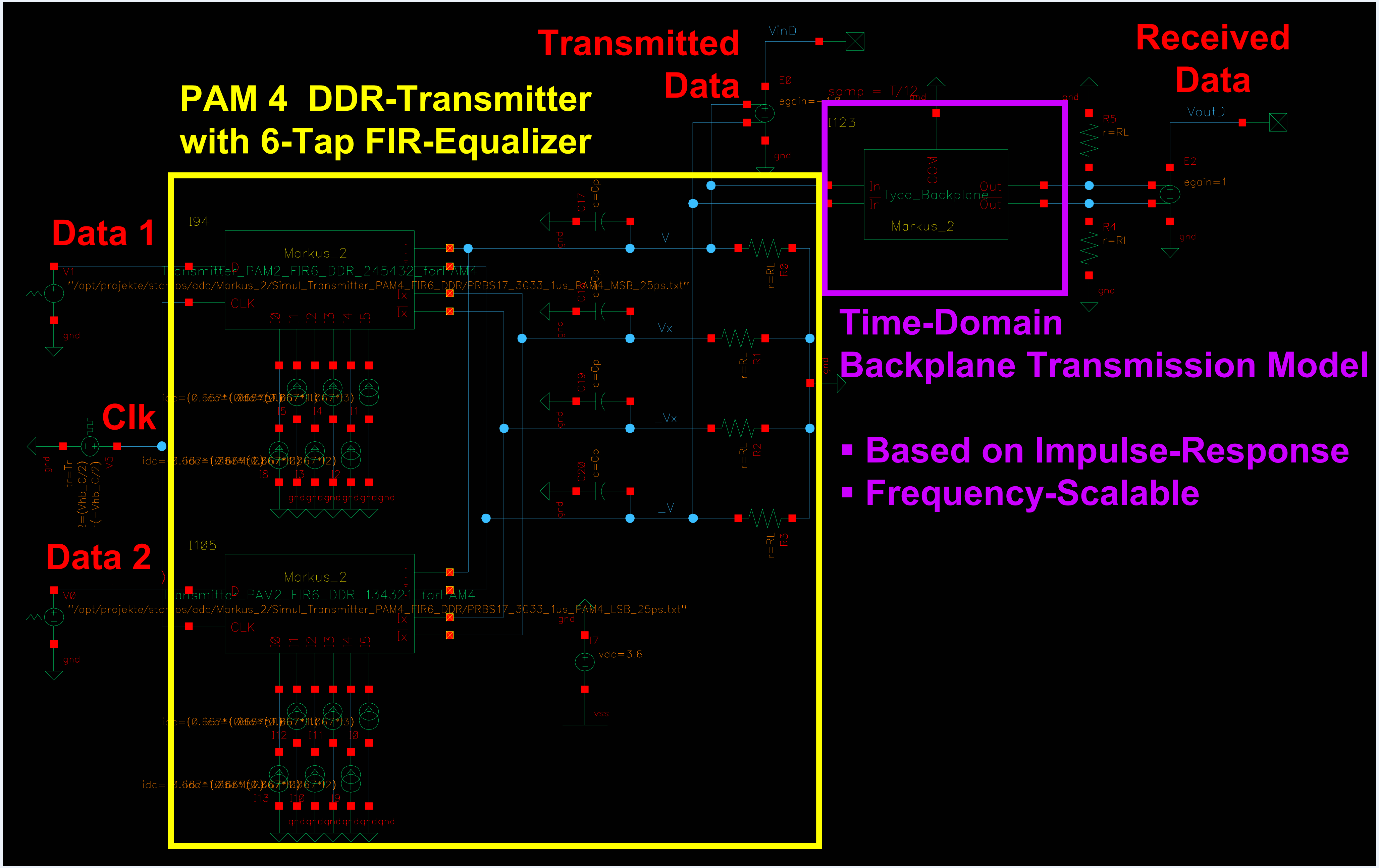
PAM 2/4 / FIR/DFE-EQ versus Insertion Loss

Bit Rate [Gbit/s]		3.33	6.67	10.0	13.33
IL @ f_{bit}/2 [dB]		**-8.9**	**-22.5**	**-27.1**	**-54.6**
Modul.	**EQ-Meth.**				
PAM 2	**none**	+/-	-	-	-
	FIR	++	+	-	-
	FIR+DFE	Overkill	++	-	-
PAM 4	**FIR**	Overkill	++	+	-
	FIR+DFE	Overkill	++	+	+

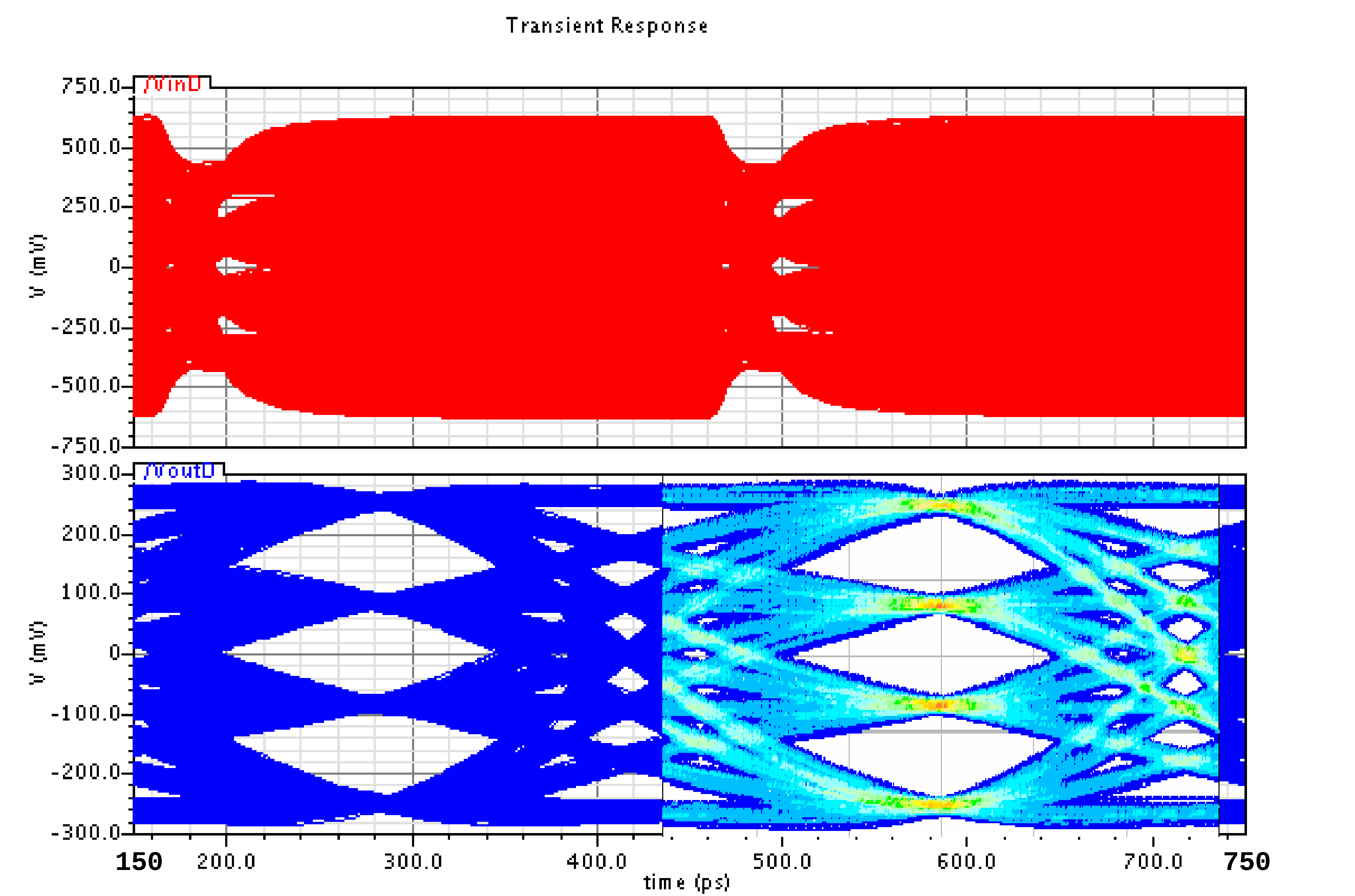
90nm-CMOS FIR-Transmitter Evaluation



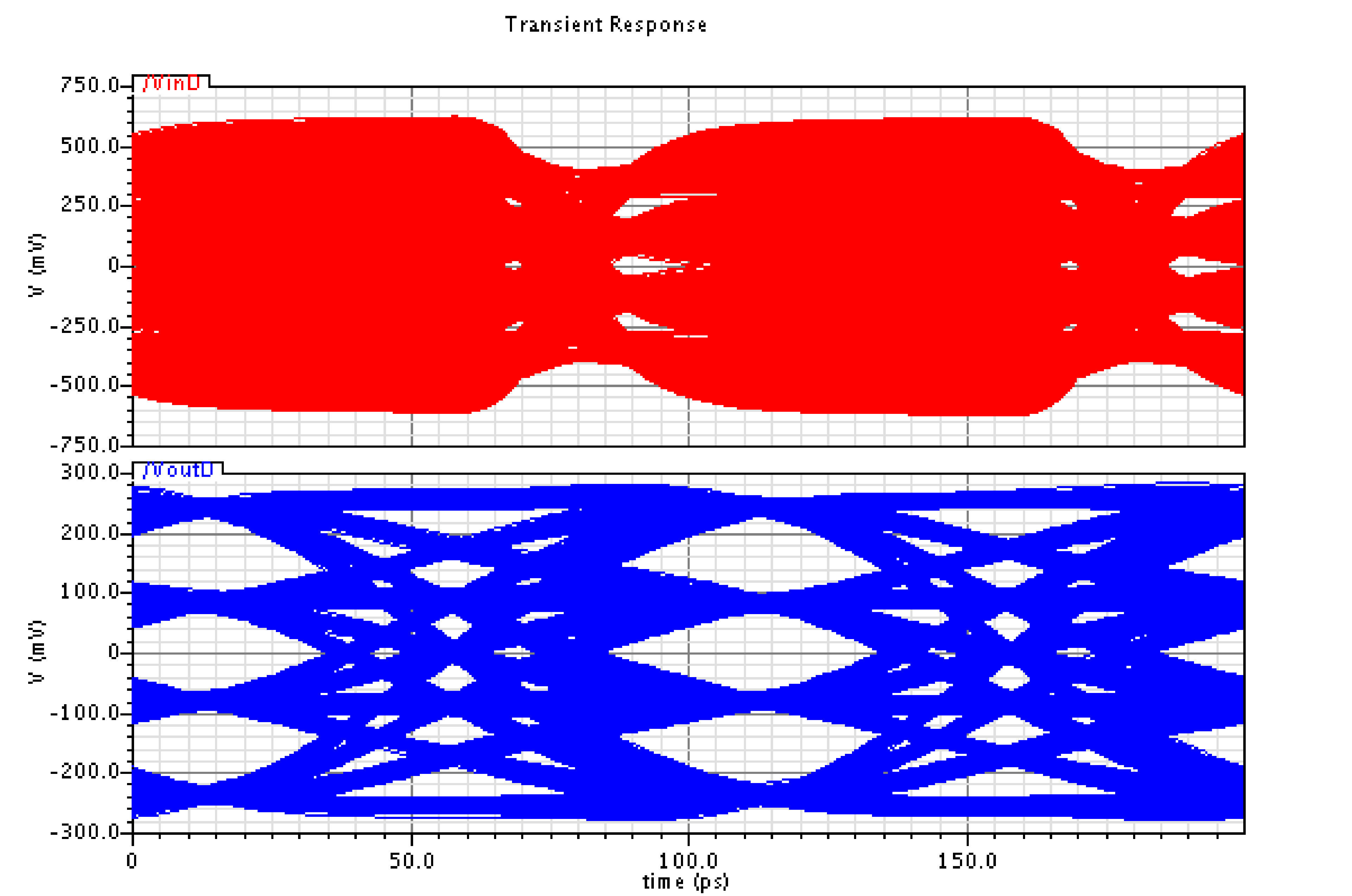
PAM 4 Test Bench with 6-Tap FIR-Equalizer in Transmitter



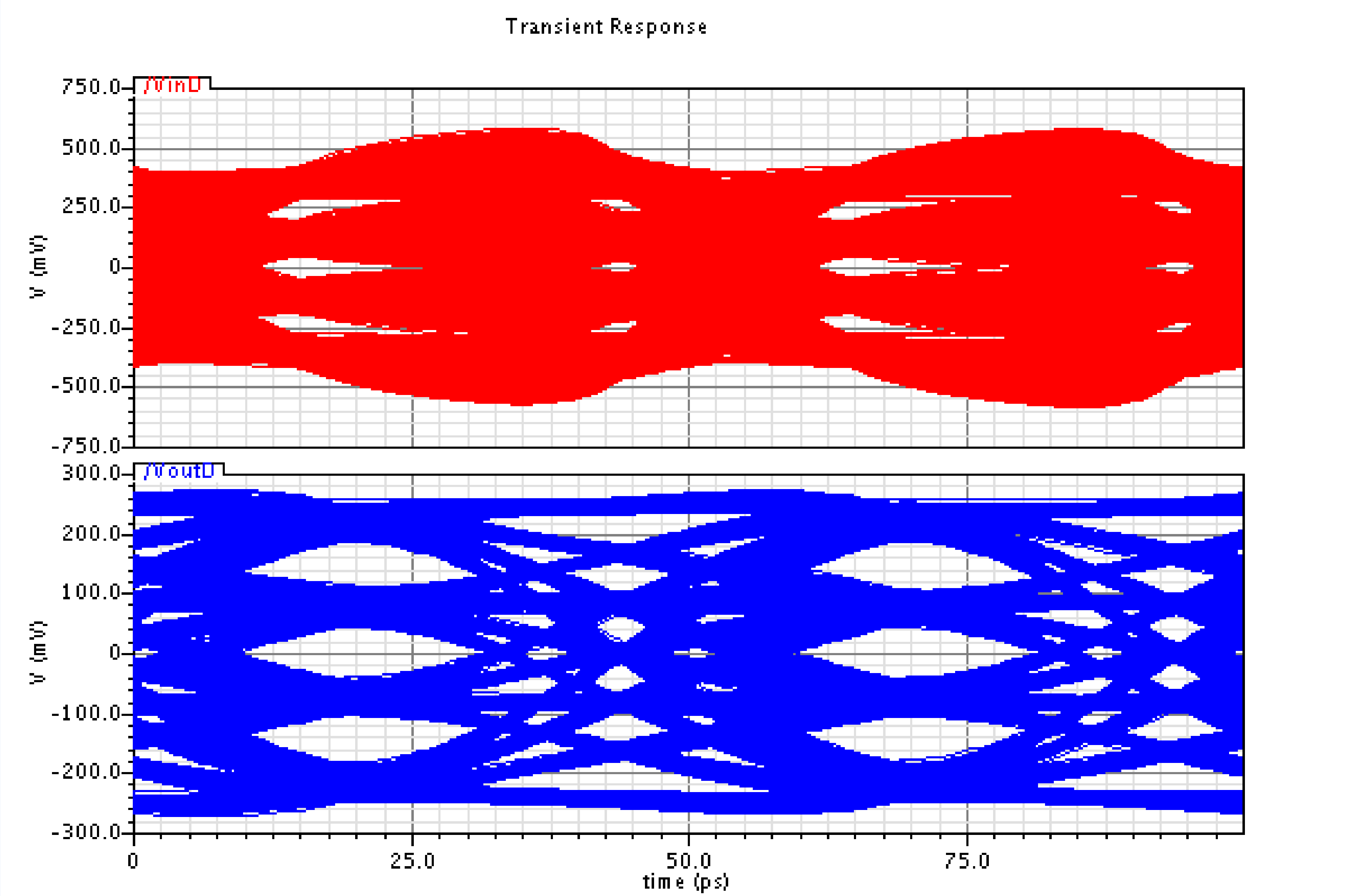
6.67 Gbit/s PAM4 (T_{sym} = 300 ps, IL @3.33 GHz = 22.5 dB)



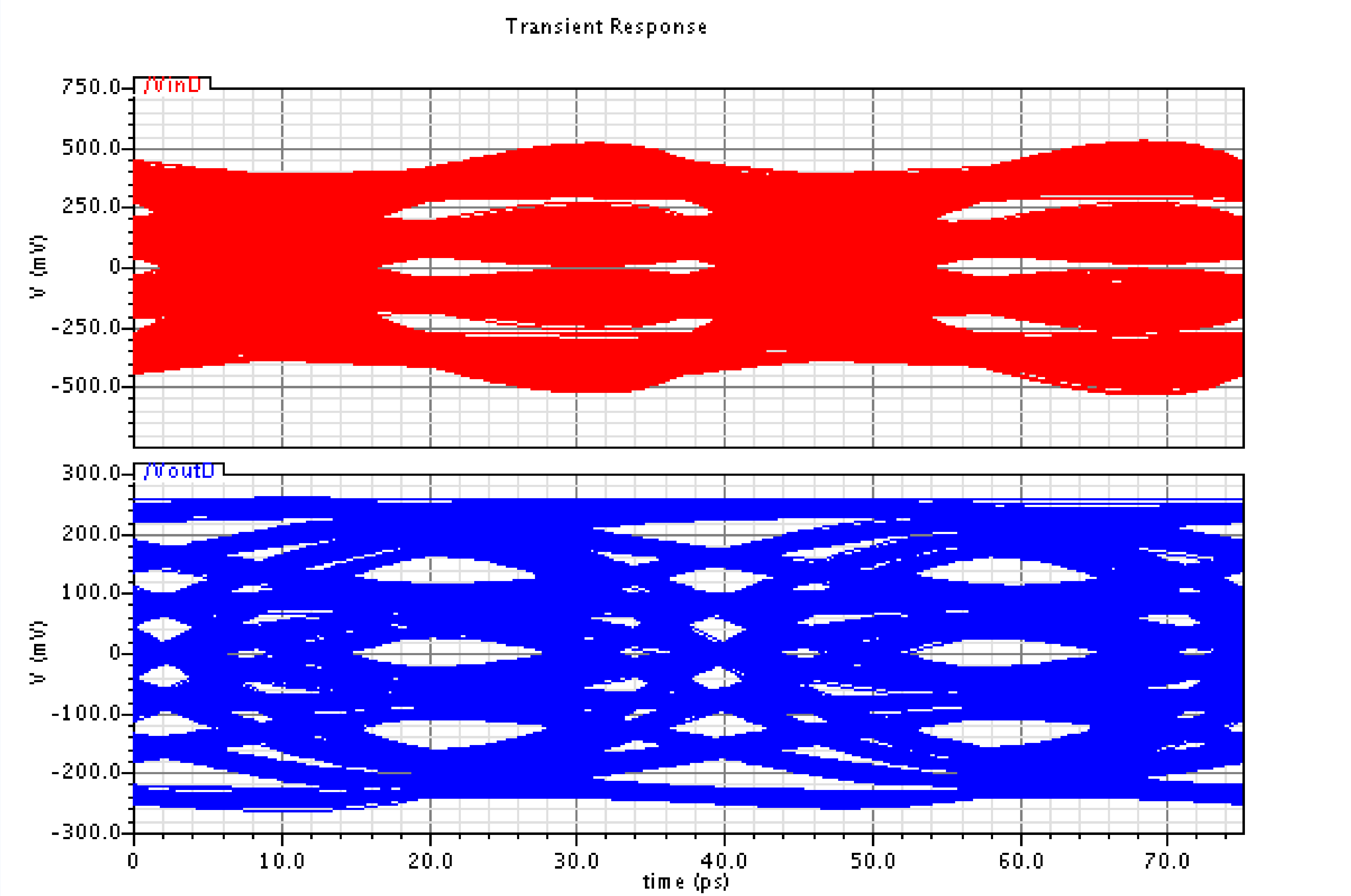
20 Gbit/s PAM4 (T_{sym} = 100 ps, IL @ 10 GHz = 22.5 dB)



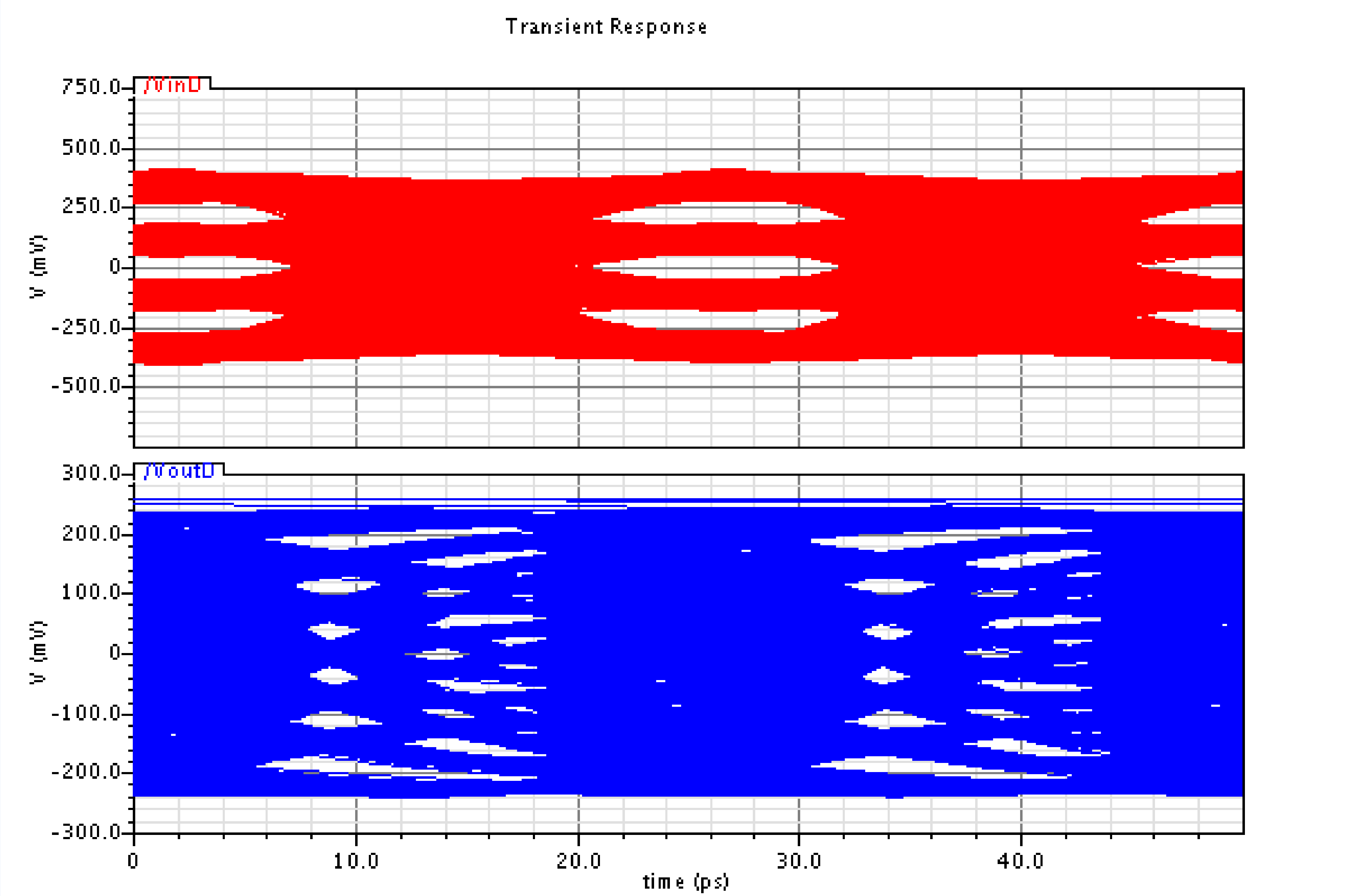
40 Gbit/s PAM4 (T_{sym} = 50 ps, IL @ 20 GHz = 22.5 dB)



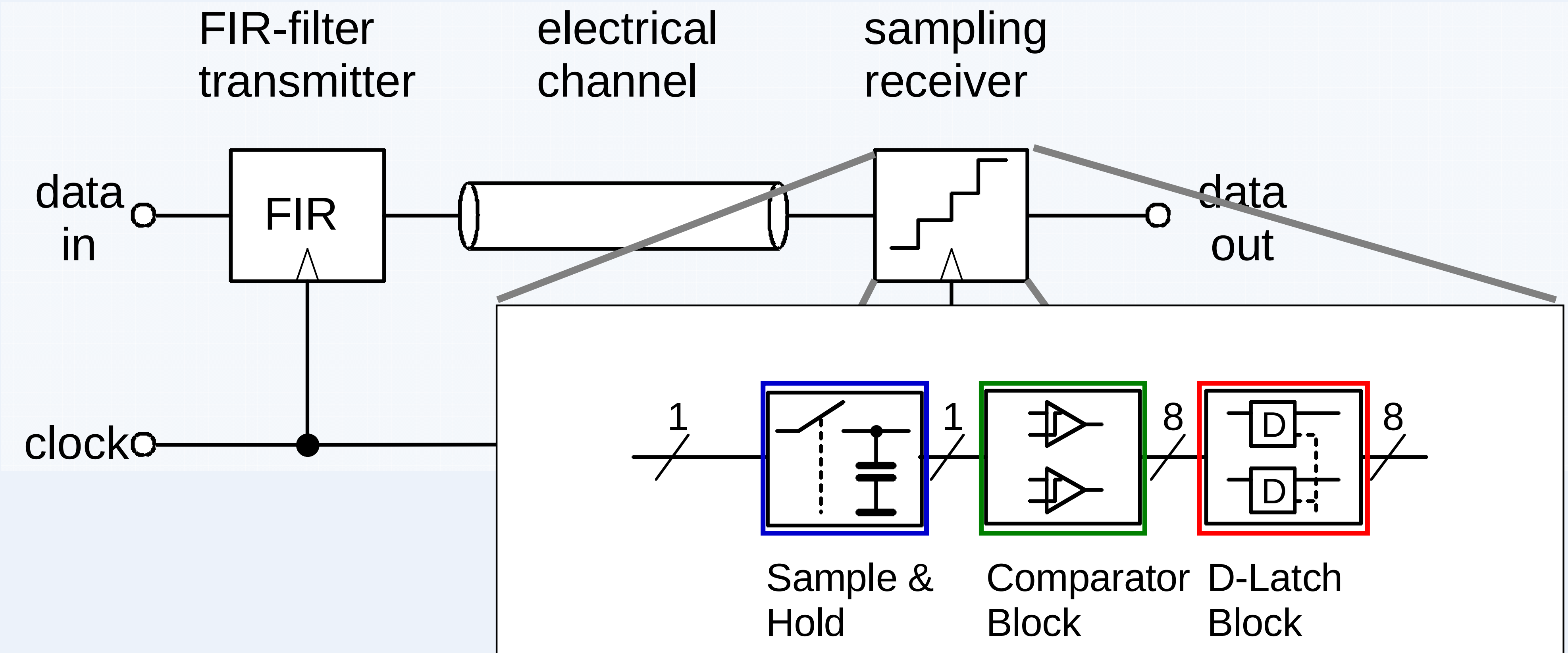
60 Gbit/s PAM4 (T_{sym} = 35.5 ps, IL @ 30 GHz = 22.5 dB)



80 Gbit/s PAM4 (T_{sym} = 25 ps, IL @ 40 GHz = 22.5 dB)



90nm-CMOS FIR-Transmitter & Sampling Receiver



Sampling:

continuous-time → discrete-time

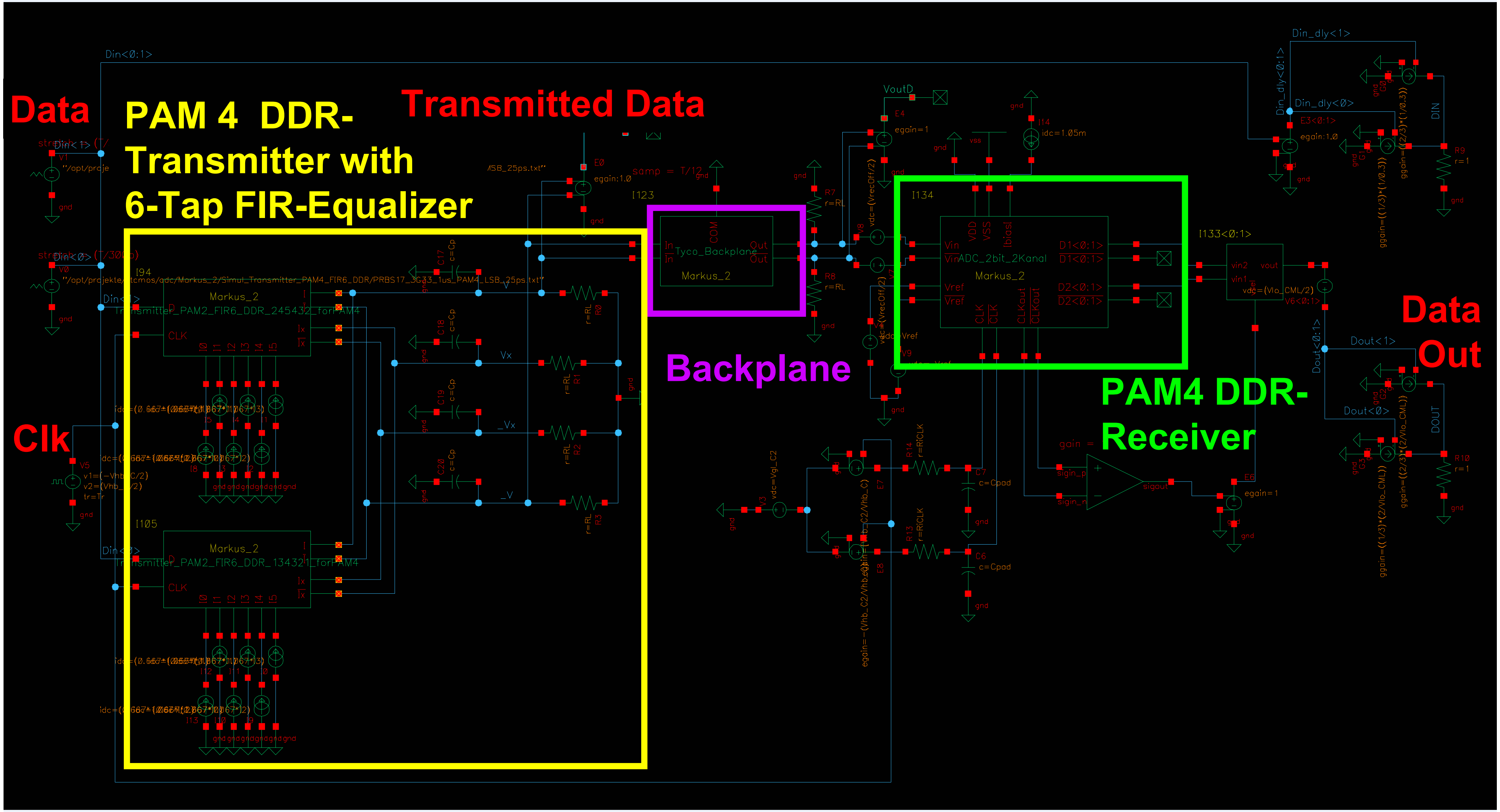
Quantization:

continuous-value → discrete-value

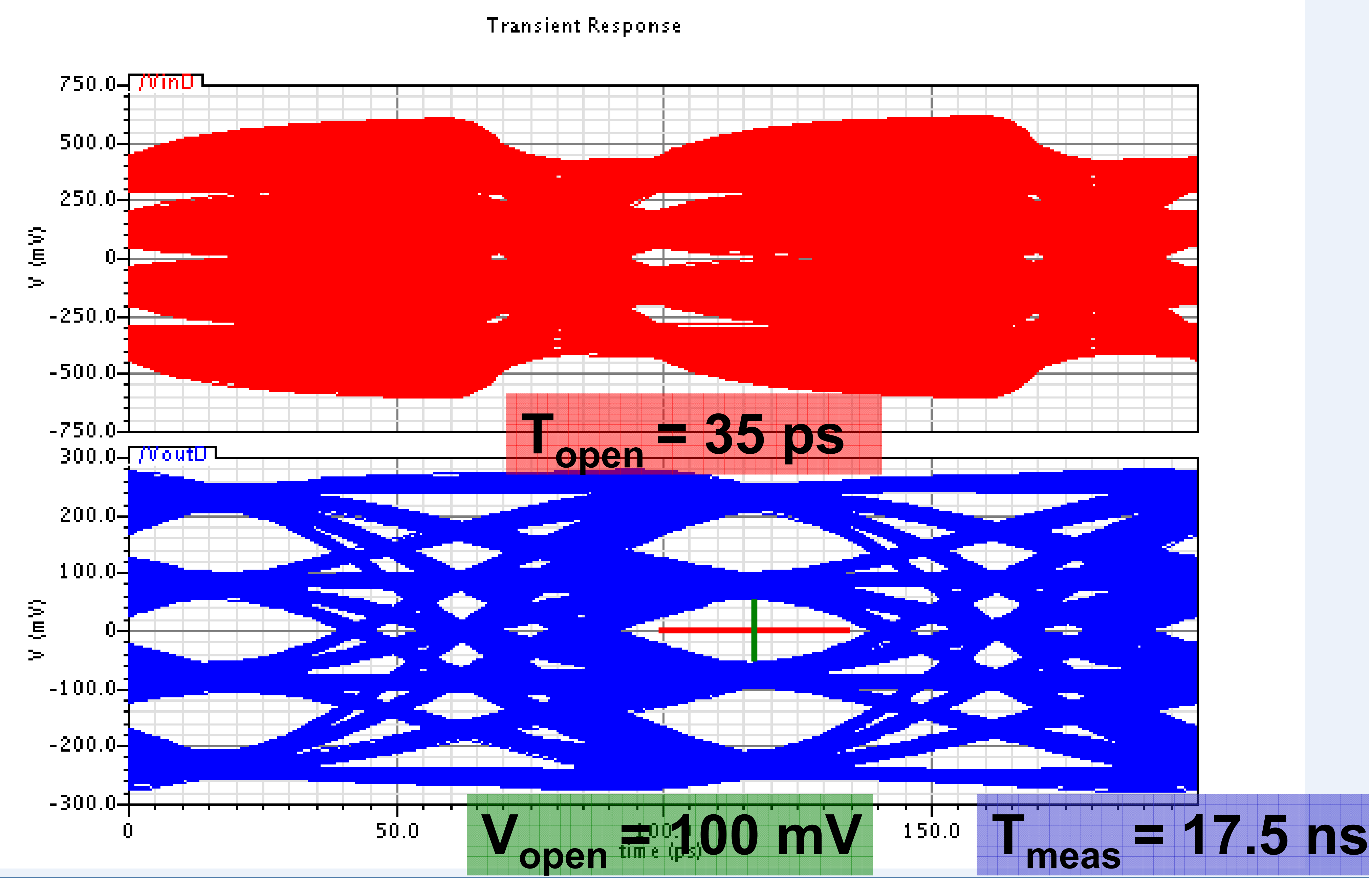
Resampling:

continuous-time → discrete-time

PAM4 Test Bench with 6-Tap FIR-Transmitter & Receiver



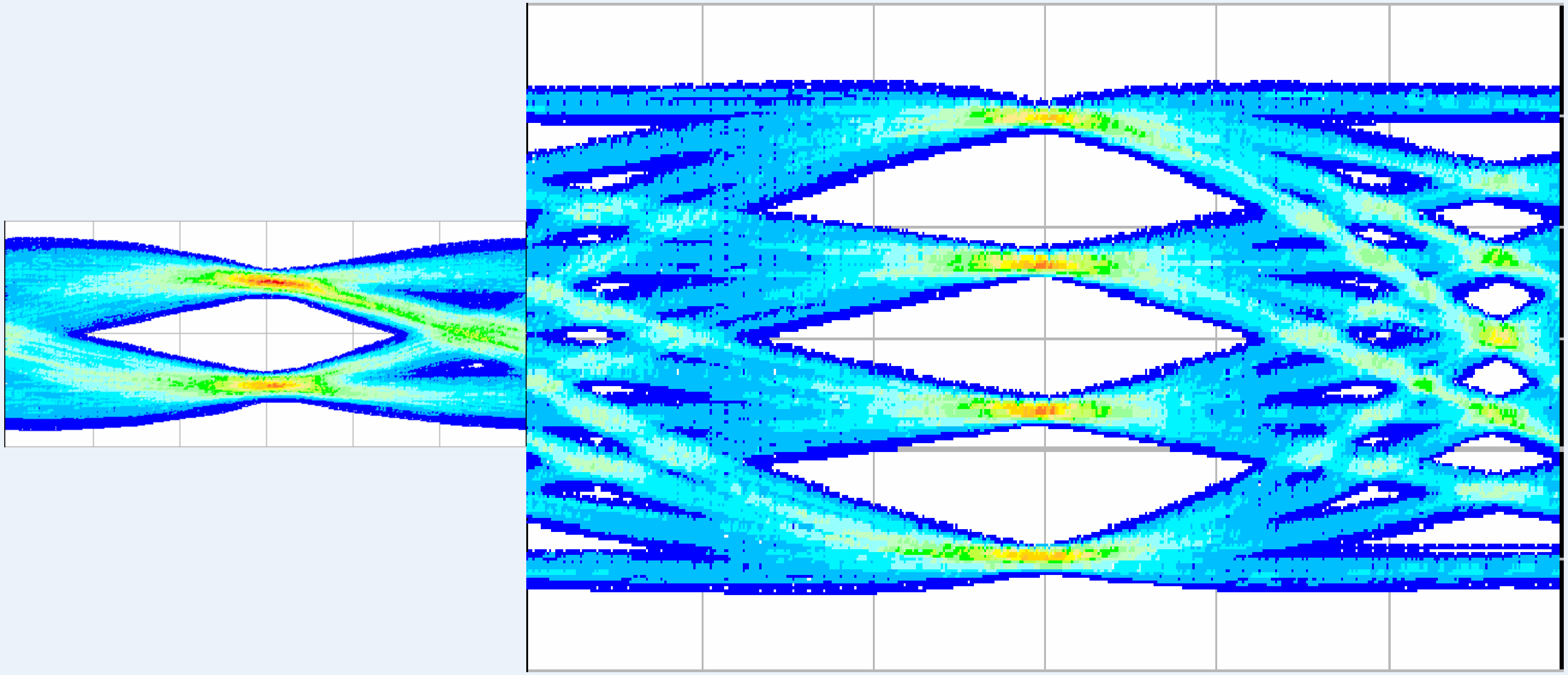
20 Gbit/s PAM4 (T_{sym} = 100 ps, IL @10 GHz = 22.5dB)



Summary IL = 22.5 dB @ $f_{bit}/2$ (w/o Receiver, 20 Gbit/s)

Quality Measure			V_{open}	T_{open}	A_{open}
EQ	Taps	PAM	[mV]	[ps]	[pVs]
FIR	2 pre 3 post	2	85	29	2.46
		4	137	46	6.30

2 - PAM

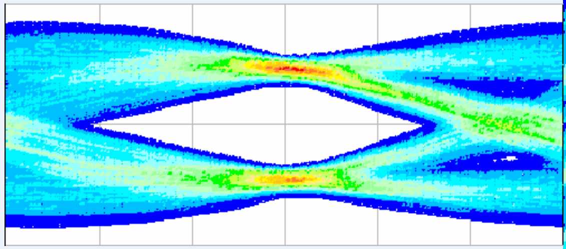


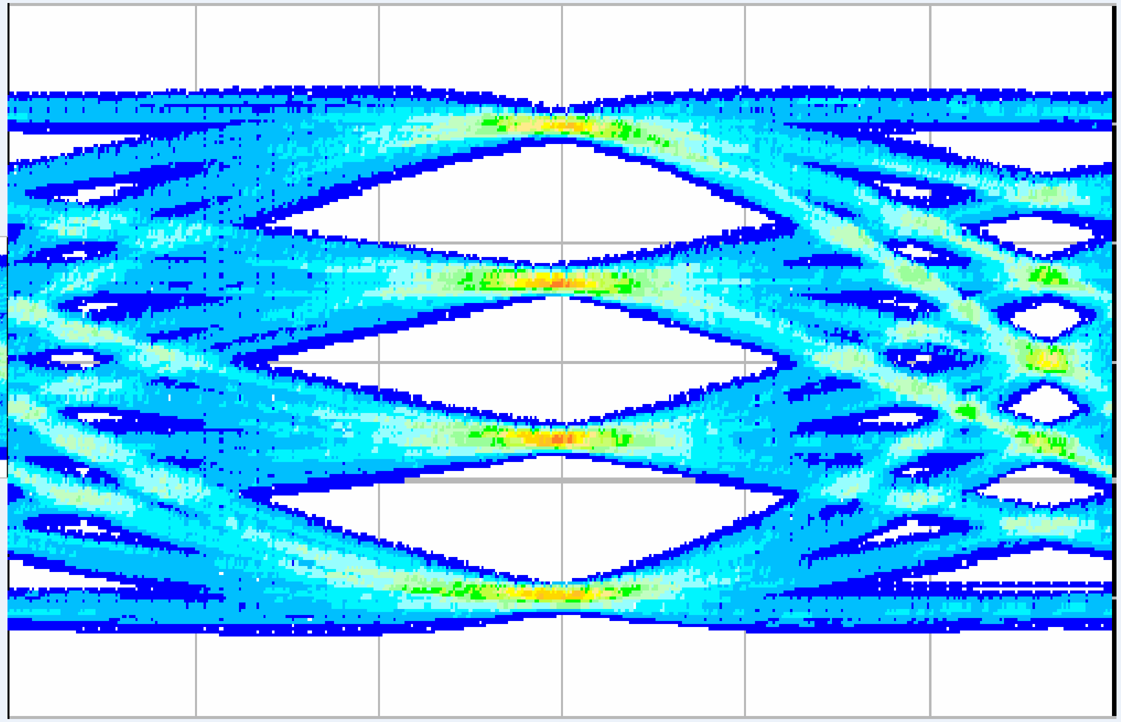
4 - PAM

Summary IL = 22.5 dB @ $f_{bit}/2$ (w/ Receiver, 20 Gbit/s)

Quality Measure			V_{open}	T_{open}	A_{open}
EQ	Taps	PAM	[mV]	[ps]	[pVs]
FIR	2 pre 3 post	2	60	29	1.8
		4	<u>100</u>	<u>35</u>	<u>3.5</u>

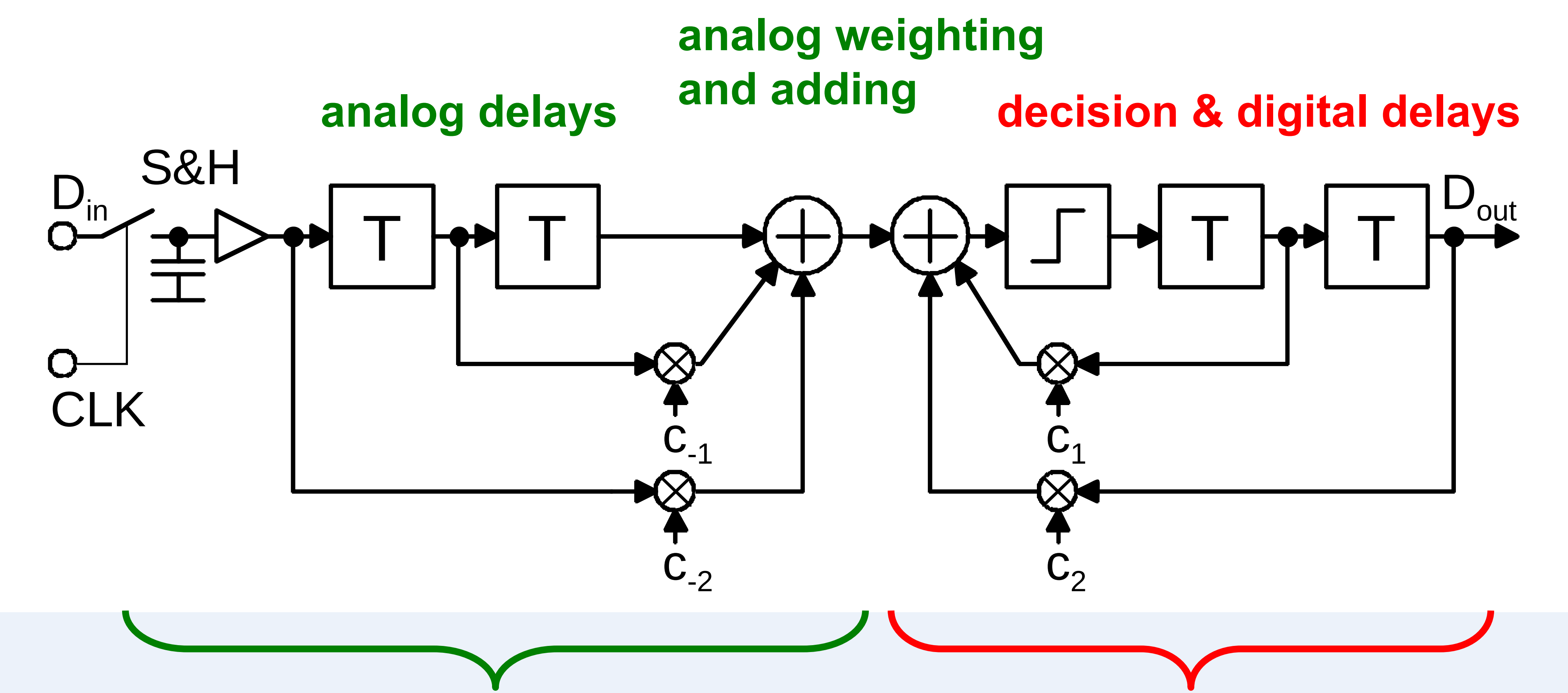
2 - PAM





4 - PAM

130nm-CMOS Sampling Receive Equalizer Concept



Finite-Impulse-Response (FIR) Filter — **removes *pre*cursor ISI**

Decision Feedback Equalizer (DFE) — **removes *post*cursor ISI**

M. Grözing, B. Philipp, M. Neher, M. Berroth, “Sampling Receive Equalizer with Bit-Rate Flexible Operation up to 10 Gbit/s,” *European Solid-State Circuits Conference (ESSCIRC) 2006,* pp. 516-519, Montreux, Switzerland, September 19-21, 2006.

130nm-CMOS Equalizer Half-Rate-Implementation

full rate data input
half rate clock

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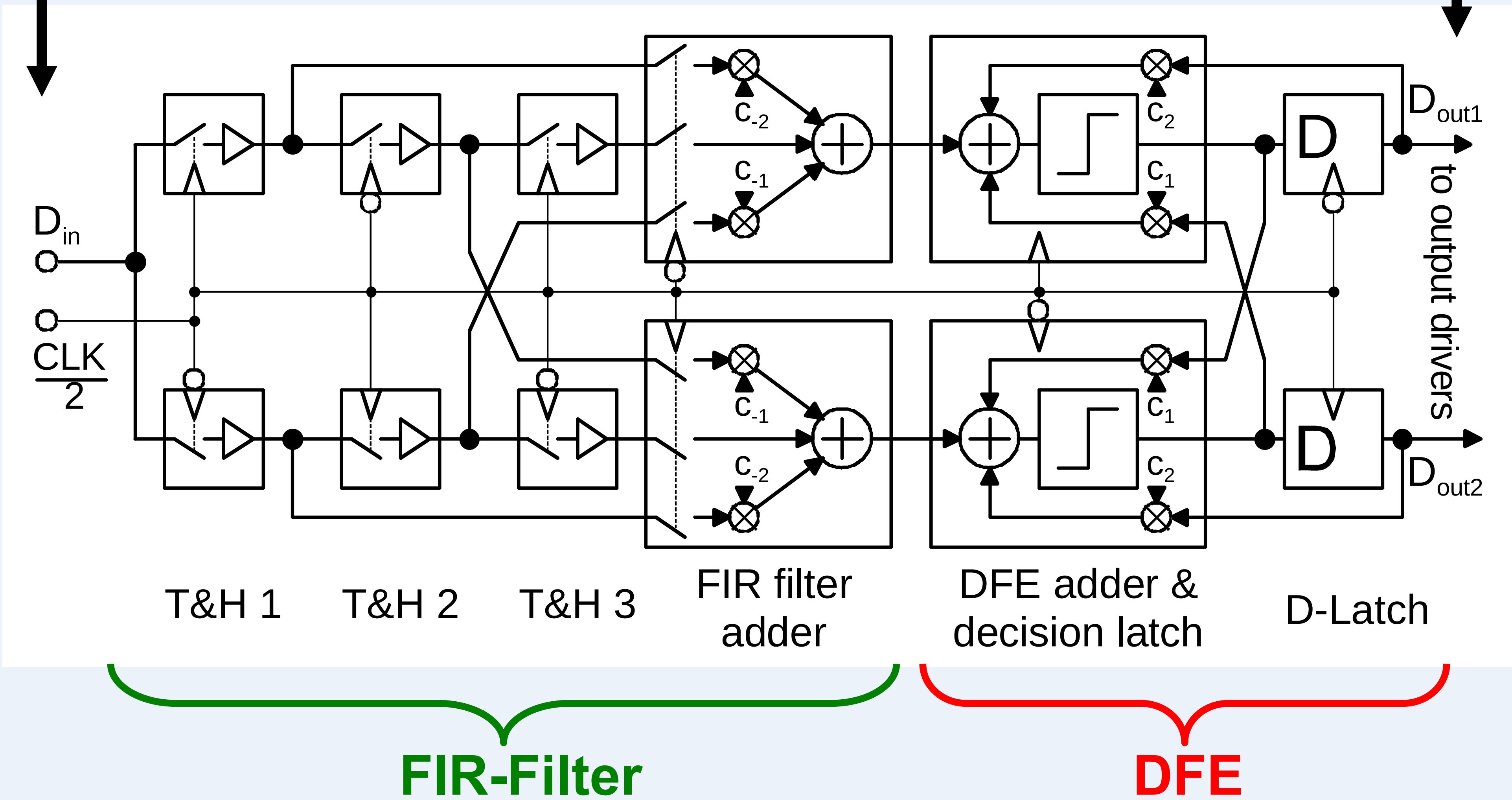
half rate demultiplexed data outputs



130nm-CMOS Equalizer Chip Photograph

Input:
max. 10 Gbit/s

M. Grözing, B. Philipp, M. Neher, M. Berroth,
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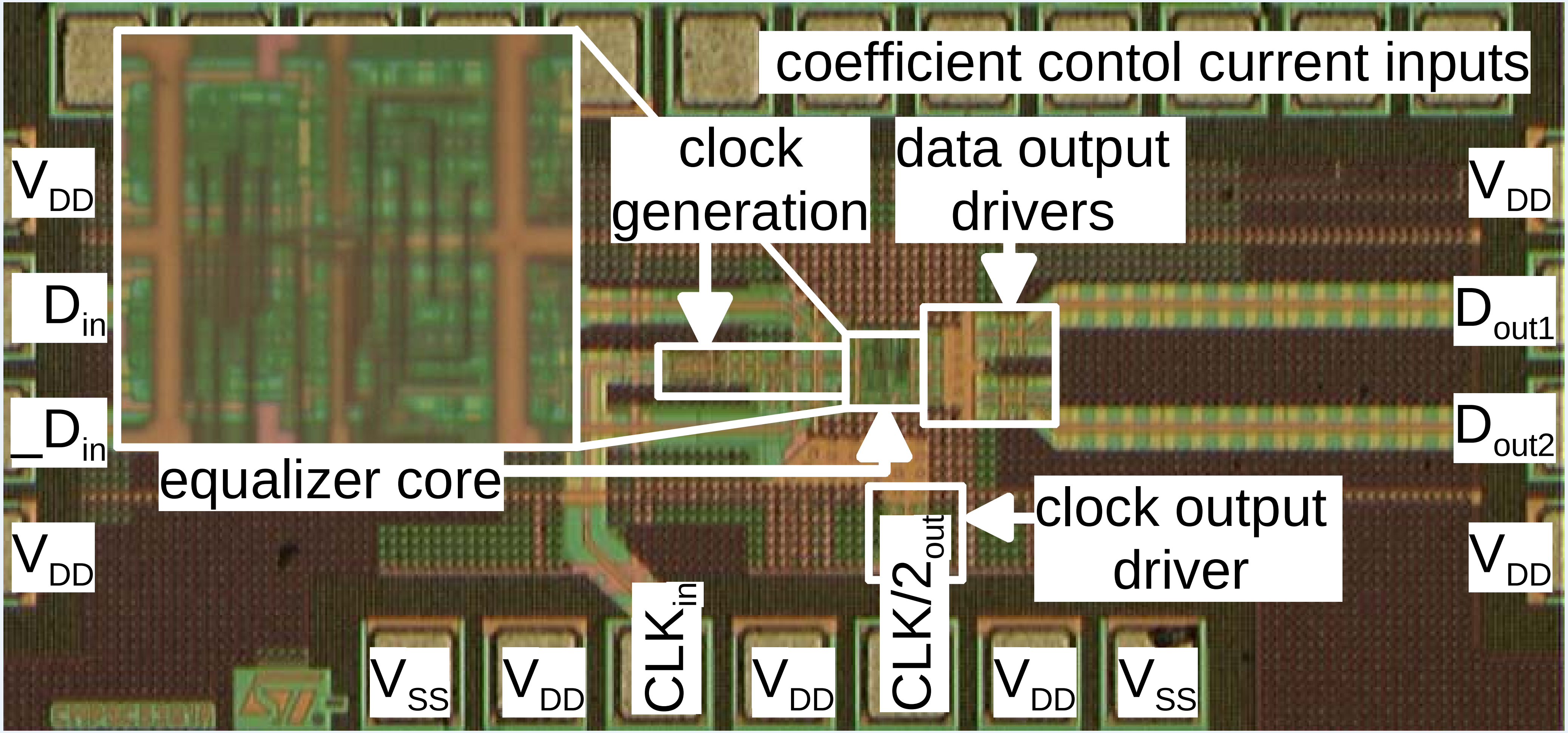
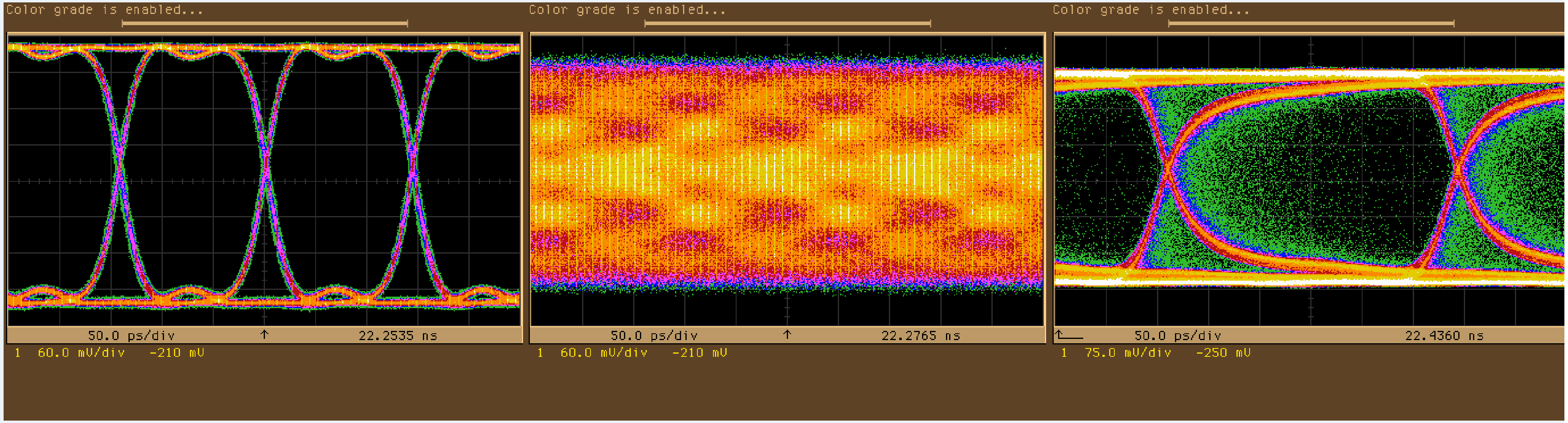
Output:
max. 2x 5 Gbit/s

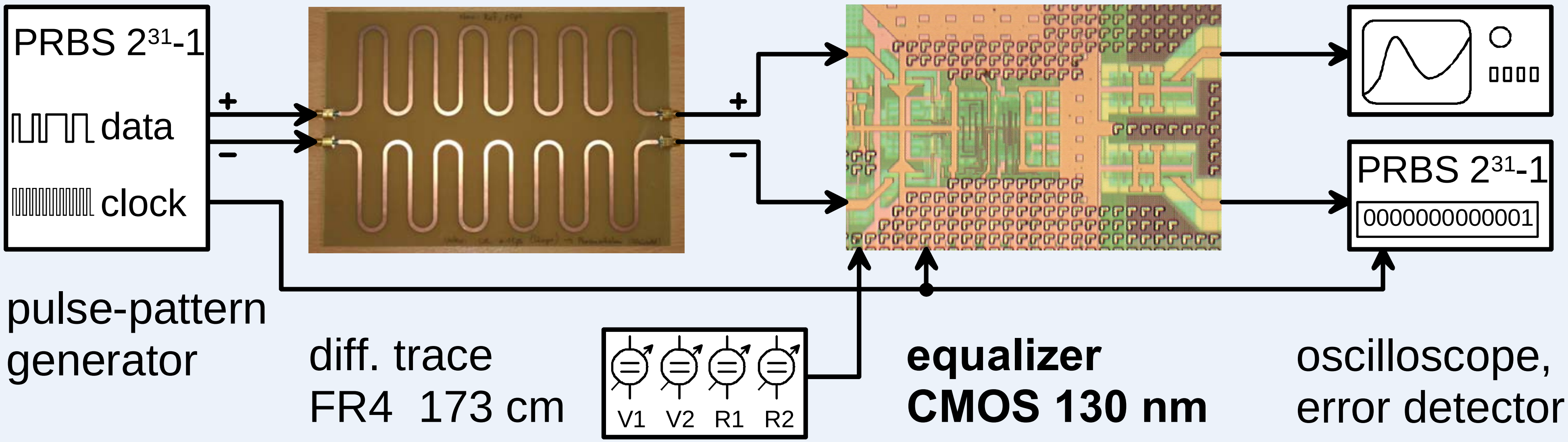


Chip area: 1400 µm x 600 µm
Core area: 60 µm x 56 µm

Experimental Results (1): 7 Gbit/s over 173 cm FR4



7 Gbit/s | 7 Gbit/s | 2x 3.5 Gbit/s



Loss: 24 dB @ 3.5 GHz

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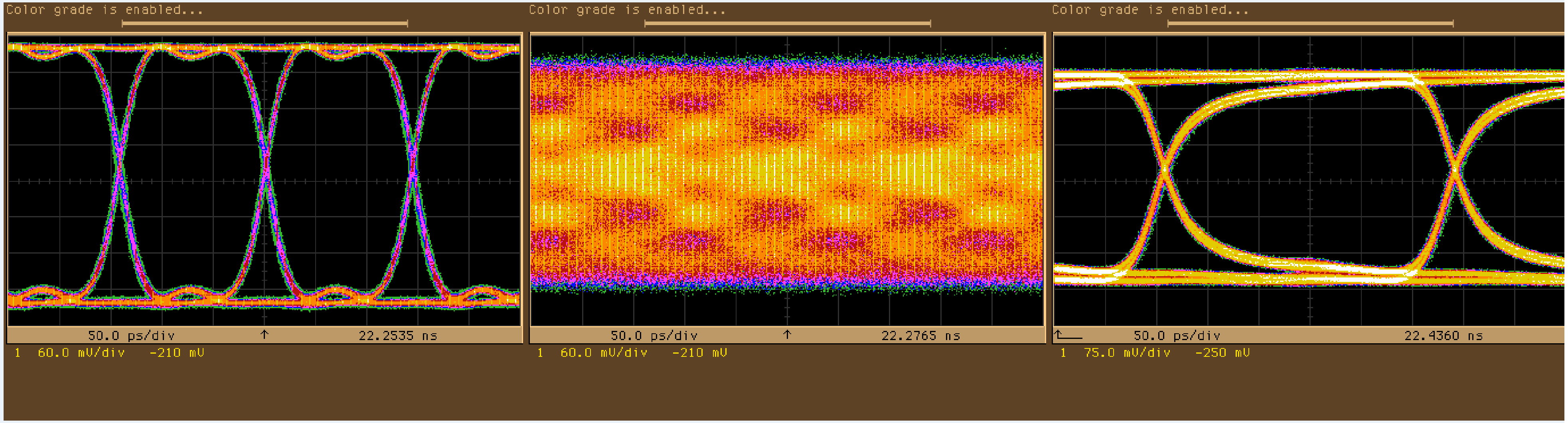
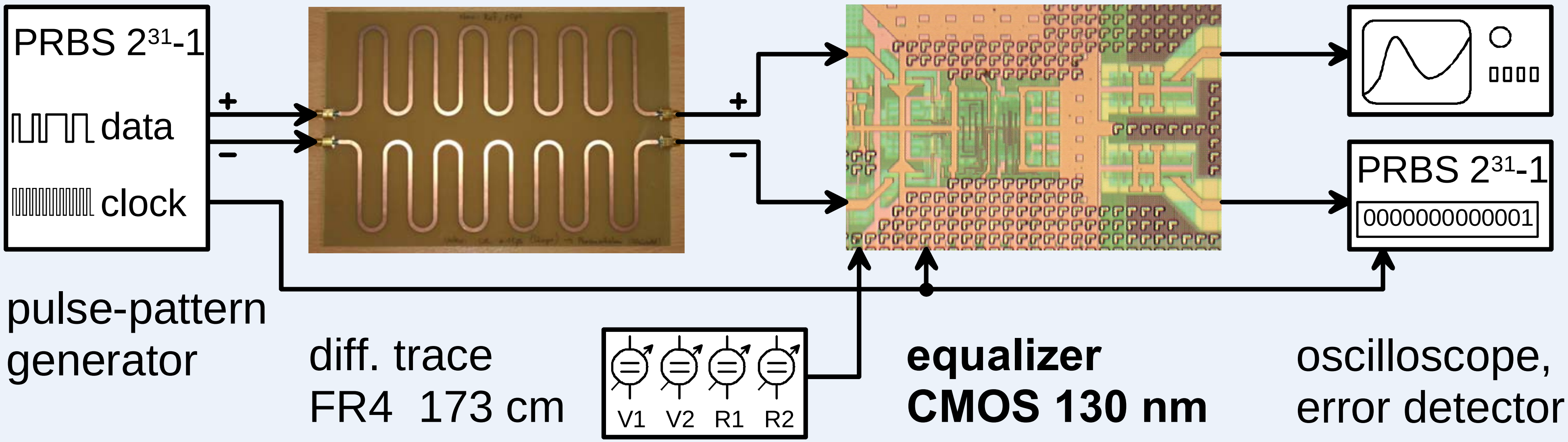
Experimental Results (1): 7 Gbit/s over 173 cm FR4



7 Gbit/s | 7 Gbit/s | 2x 3.5 Gbit/s



coefficient control

Loss: 24 dB @ 3.5 GHz

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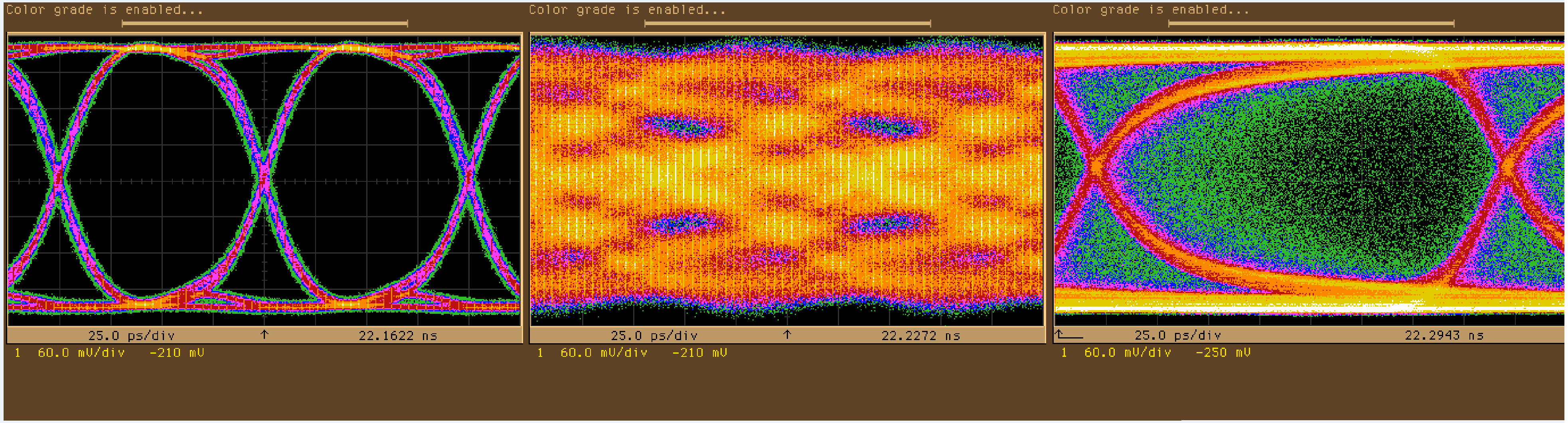
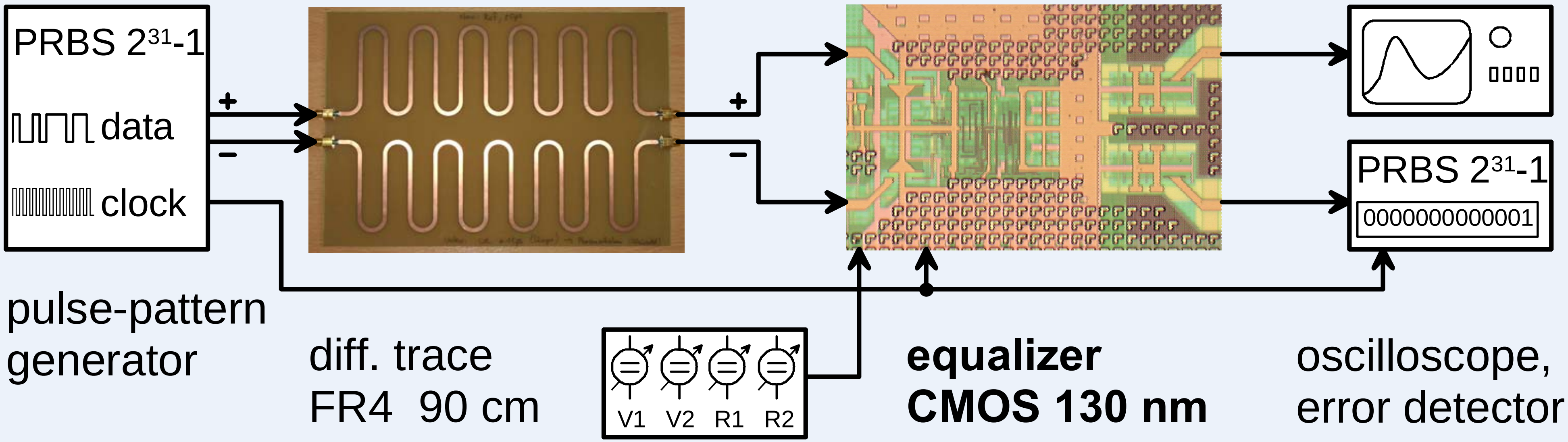
pp. 516-519, Montreux, Switzerland, September 19-21, 2006.

Experimental Results (2): 10 Gbit/s over 90 cm FR4



10 Gbit/s | 10 Gbit/s | 2x 5 Gbit/s



Loss: 18 dB @ 5 GHz

coefficient control

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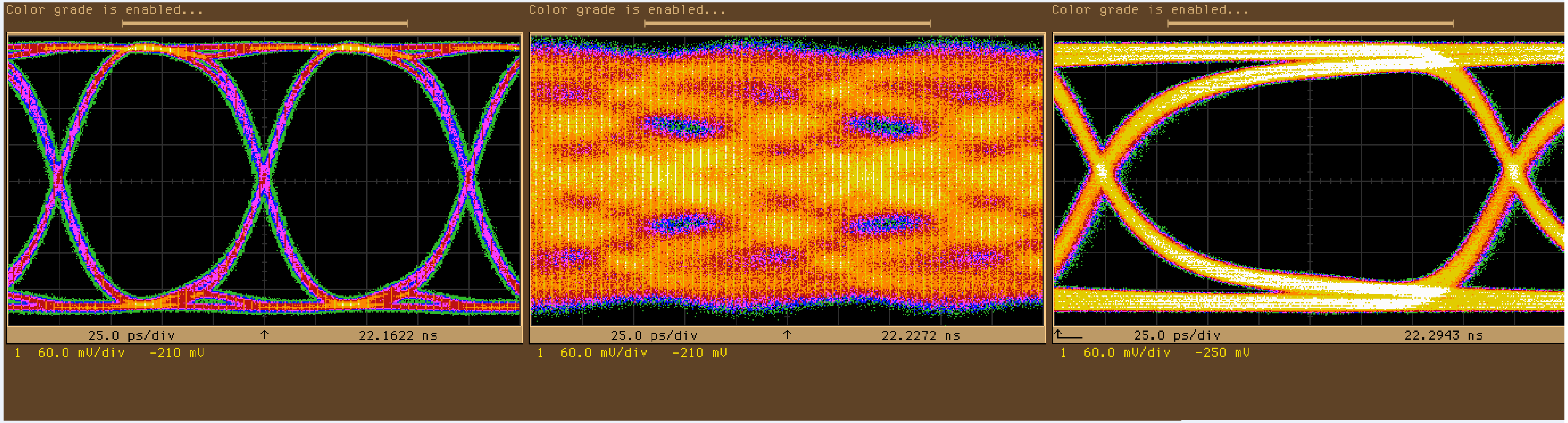
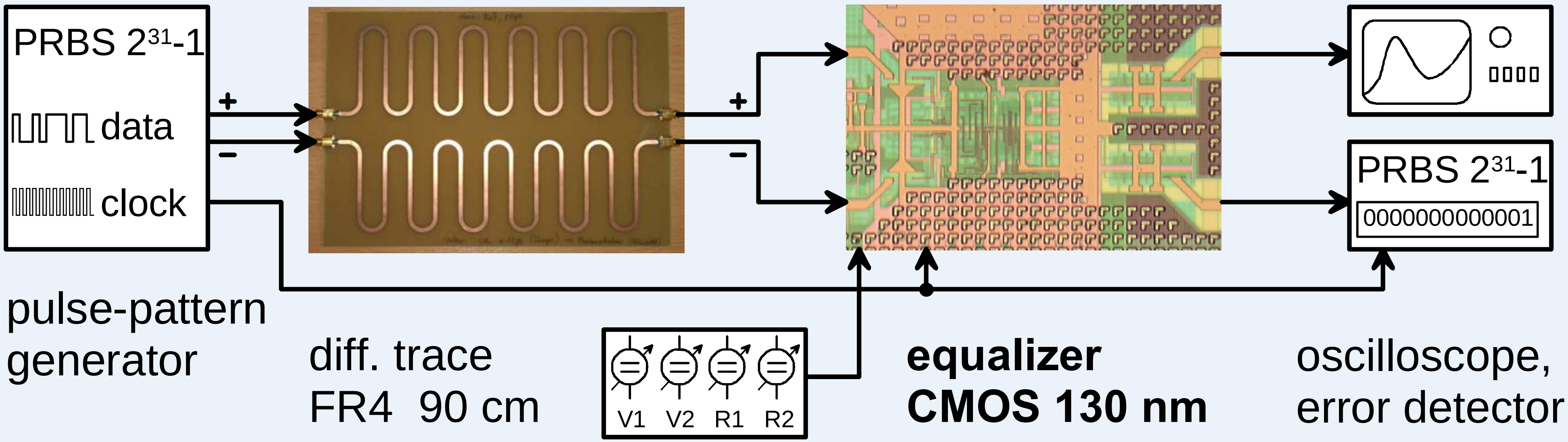
Experimental Results (2): 10 Gbit/s over 90 cm FR4



10 Gbit/s | 10 Gbit/s | 2x 5 Gbit/s



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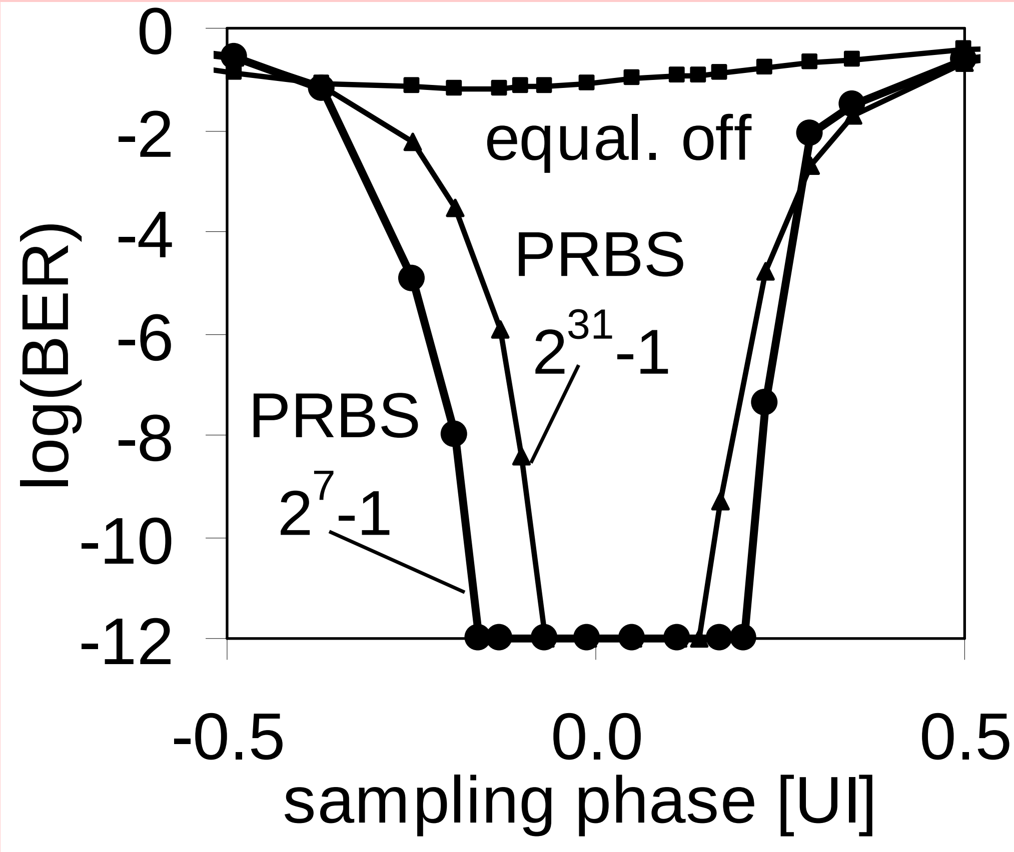
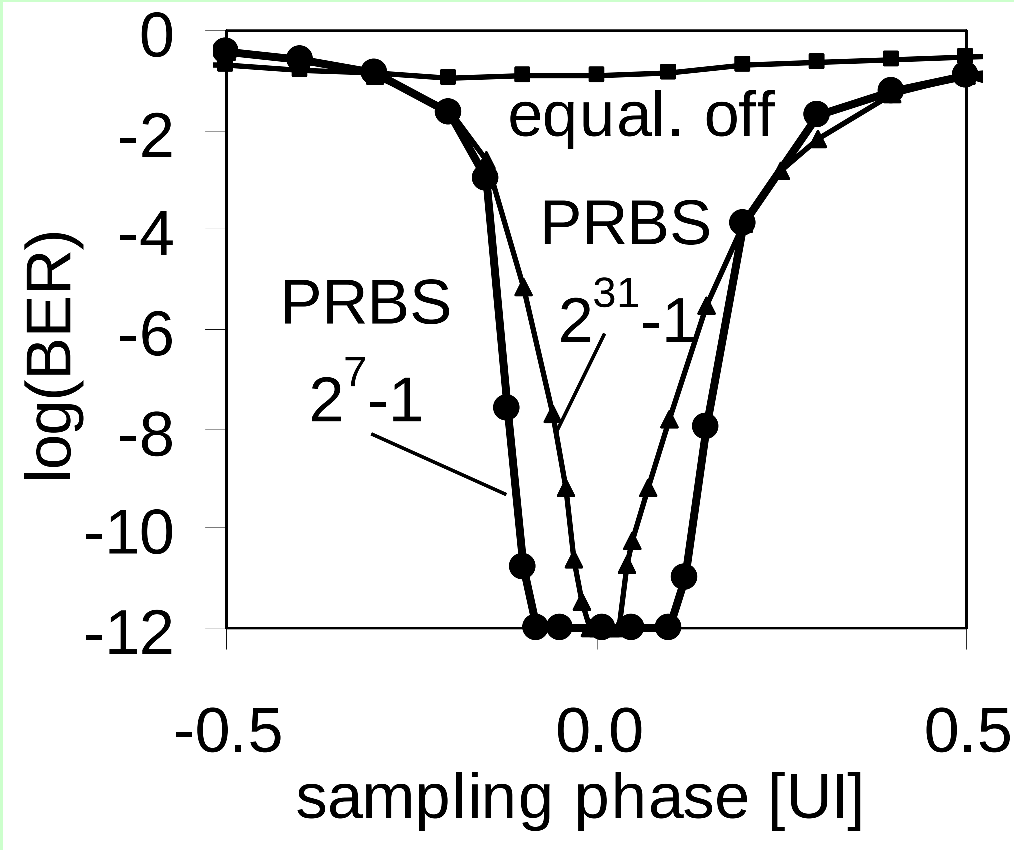
Experimental Results: BER versus Sampling Phase





173 cm FR4 trace @ 6 Gbit/s

Loss: 19 dB @ 3 GHz

90 cm FR4 trace @ 10 Gbit/s

Loss: 18 dB @ 5 GHz

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130nm-CMOS Equalizer Performance Summary

supply voltage V_{DD}	1.3 V	P_{DC} equalizer core*	21 mW
maximum bit rate f_{max}	10 Gbit/s	P_{DC} clock generator**	33 mW
minimum bit rate f_{min}	0.5 Gbit/s	P_{DC} total (with drivers)	200 mW
max. poss. channel loss for BER < 10^{-12}, PRBS 2^{31}-1, 7 Gbit/s			24 dB
min. $V_{pp,PPG}$ for BER < 10^{-11}, PRBS 2^{7}-1, 10 Gbit/s, 90 cm FR4			300 mV
min. $V_{pp,PPG}$ for BER < 10^{-11}, PRBS 2^{7}-1, 6 Gbit/s, 173 cm FR4			230 mV

*circuitry corresponding to slide 8; **circuitry in dashed box of slide 13.

M. Grözing, B. Philipp, M. Neher, M. Berroth,
"Sampling Receive Equalizer with Bit-Rate Flexible Operation up to 10 Gbit/s,"
European Solid-State Circuits Conference (ESSCIRC) 2006,
pp. 516-519, Montreux, Switzerland, September 19-21, 2006.

Summary

- **System Level Evaluation of Doubled Data Rate Transmission on legacy BP (3.33 Gbit/s → 6.67 Gbit/s, IL = 8.9 dB @ 1.67 GHz / 22.5 dB @ 3.33 GHz)**
  - **Equalization is a must for both PAM2 & PAM4-transmission**
  - **PAM4 offers larger eye area with less equalization effort**
- **DDR PAM2/4 Transmitter & Receiver Evaluation in 90nm CMOS**
  - **PAM 2/4 6-Tap FIR-EQ-DDR-Transmitters** work up to **40 Gbit/s**
  - **PAM 2/4 Receivers** work up to **20 Gbit/s,**
    Eye Diagram Margins indicate that they work up to **40 Gbit/s**
  - **PAM 4 show's a clear advantage in receiver eye area (~ factor 2 to 3)**
- **Receive-Side FIR-DFE-Equalizer for up to 10 Gbit/s in 130nm CMOS**
  - **small chip area (core: 60 µm x 56 µm)**
  - **low power consumption (core: 21 mW, clock: 33mW)**
  - **up to 24 dB channel loss compensation**
  - **no spiral inductors**
  - **bit-rate flexible operation**
  - **Patent situation:**
    - **DE 10 2006 034 033 B3 patent granted**
    - **PCT patent application pending**
    - **License request to Technologie-Lizenz-Büro (TLB), www.tlb.de**